THE pcb design MAGAZINE

July 2016

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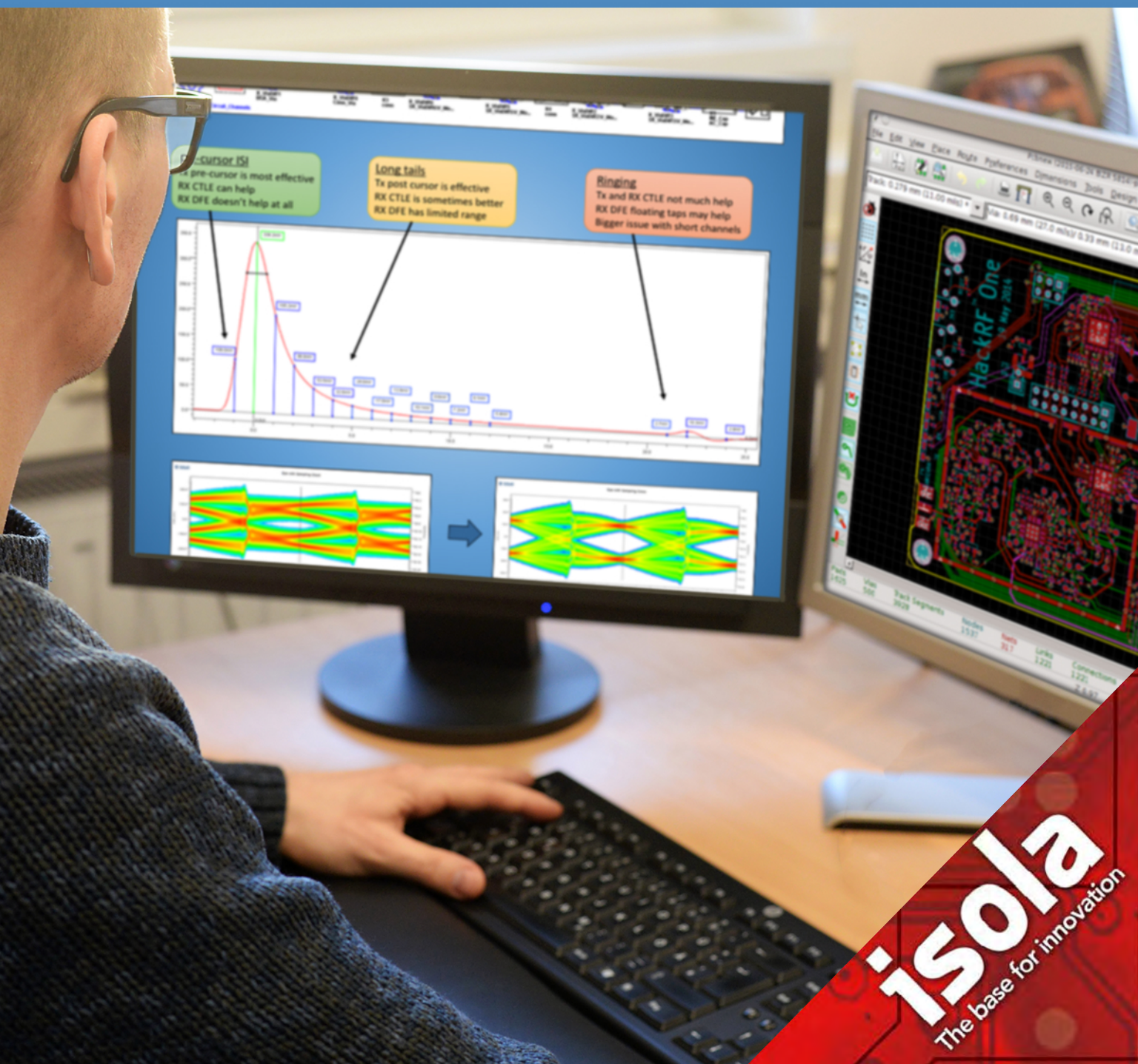
THE SIGNAL INTEGRITY ISSUE



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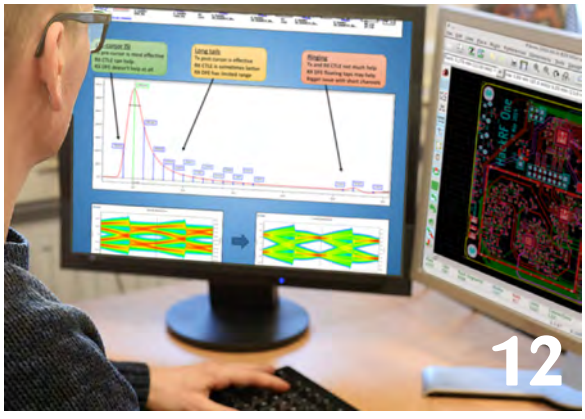

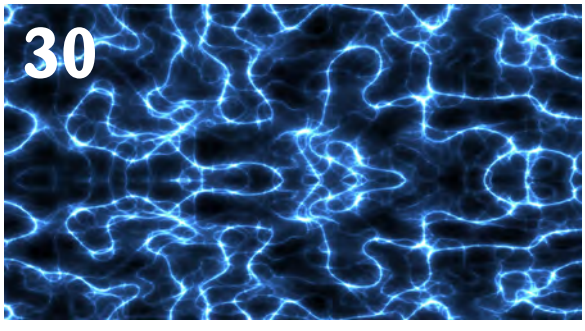

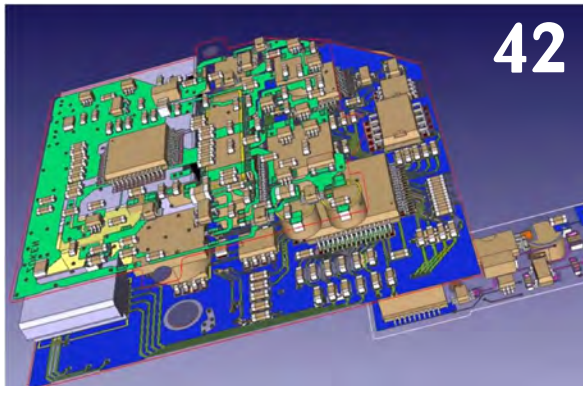

The Signal Integrity Issue

As the not-so-old saying goes, "If you don't have signal integrity issues yet, you will." This month we bring you a variety of SI articles, starting with our cover story by Michael Steinberger and Barry Katz of SiSoft, and Donald Telian of SI Guys. We also have feature articles by Dennis Nagle of Cadence Design Systems and Narayanan TV of Zuken, as well as a feature column by Abby Monaco of Intercept Technology. Finally, we have a great interview with American Standard Circuits' John Bushie.

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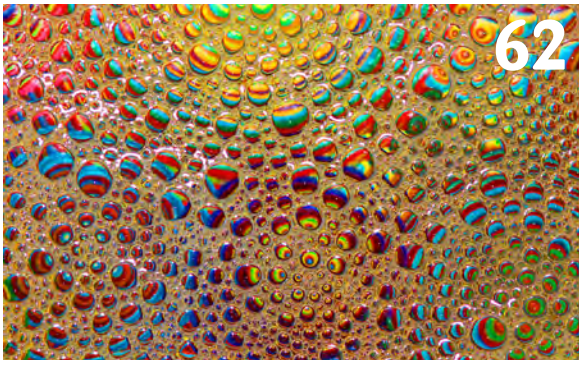

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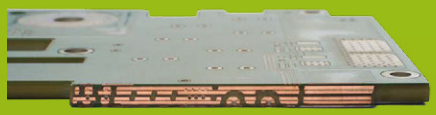

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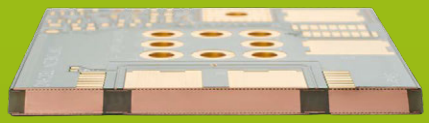

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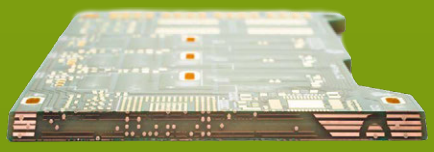

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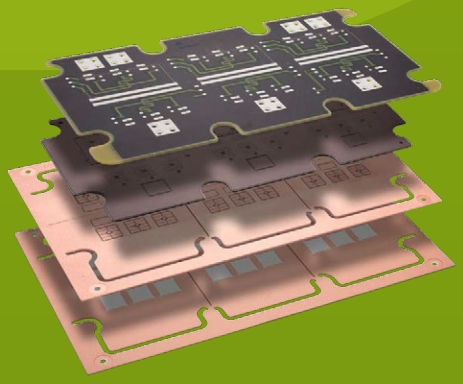

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We Want Your PCB Design Tips!

by Andy Shaughnessy
I-CONNECT007

One of the most interesting things I've noticed about the PCB design community is that it's spread out among so many different segments of the electronics industry. You all work in a vertical occupation, but it's located across a very horizontal group of companies around the world.

As a result, PCB design information is often as spread out as PCB designers are. Fortunately, designers can now access design instruction through a variety of conferences, trade shows, and webinars. But there isn't really a centralized database for design information that's useful immediately—simple design tips that a designer can use on the next design.

We want to change that.

Soon, we'll be launching *Design Tips,* an ongoing feature that will be driven by input from PCB designers and design engineers. We want to hear from readers like you. Now is the time to make your voices heard.

Do you have a handy design technique that you utilize on almost every job? Did you discover a trick or two about your software that the rest of the design community might not be aware of? We want to hear these tips and so do your design colleagues.

Send us your favorite design tips, tricks and techniques. This information can encompass any area of PCB design or design engineering:

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Keep your *Design Tips* entries short and sweet—no more than 100 words. Tool-specific tips are welcome, but keep them positive. We can't publish any tips anonymously; each tip will be published with your name, title and the name of your company. If you absolutely cannot use your company name, we'll need to have your city, state, or country if you're located outside the U.S.

We'll publish a new tip every few days, and readers will be able to see all of the previous tips as well. We see this as much more than a database; this will be a continuously updated knowledge base of useful tips that other designers can use immediately. After all, most designers know how to design a PCB. It's the little tricks that can help you save a few minutes here, and a few dollars there.

Now is your chance to share your knowledge with your colleagues, or just show off your great ideas. To submit your contribution to *Design Tips,* click here.

The Signal Integrity Issue

This month, we focus on a topic that most of you have to contend with every day, or you will eventually: signal integrity. We have a variety of articles for your perusal, starting with our cover story "New SI Techniques for Large System Performance Tuning," a paper that was presented at DesignCon 2016. Authors Michael Steinberger and Barry Katz of SiSoft, and Donald Telian of SI Guys present some brand-new techniques for equalization tuning and discontinuity reduction in large systems—techniques that can improve your design margin. Dennis Nagle of Cadence Design Systems explains how a modern constraint-driven approach can enables all teams to get involved with signal and power integrity earlier in the process. Narayanan TV of Zuken discusses some common design mistakes that can affect signal integrity, and some new solutions that can address these issues.

Next, columnist Abby Monaco of Intercept Technology takes us on her journey to more fully understand the ins and outs of impedance. We also have a great interview with John Bushie of American Standard Circuits, who explains how PCB designers can avoid over-materializing their designs by utilizing solid design for profitability (DFP) methods.

We have some great content lined up for you over the next few months. And before you know it, it will be show time again. In the meantime, it's 90° here in Atlanta, which means it's time for some sweet tea. See you next month.

PCBDESIGN

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 16 years. He can be reached by clicking here.

A Little Impurity Makes Nanolasers Shine

Scientists at The Australian National University (ANU) have improved the performance of tiny lasers by adding impurities, in a discovery which will be central to the development of low-cost biomedical sensors, quantum computing, and a faster Internet.

Researcher Tim Burgess added atoms of zinc to lasers one hundredth the diameter of a human hair and made of gallium arsenide, a material used extensively in smartphones and other electronic devices. The impurities led to a 100 times improvement in the amount of light from the lasers.

Gallium arsenide is a common material used in smartphones, photovoltaic cells, lasers and light-emitting diodes (LEDs), but is challenging to work with at the nanoscale as the material requires a surface coating before it will produce light.

Previous ANU studies have shown how to fabricate suitable coatings.

The new result complements these successes by increasing the amount of light generated inside the nanostructure, said research group leader Professor Chennupati Jagadish, from the ANU Research School of Physics Sciences.

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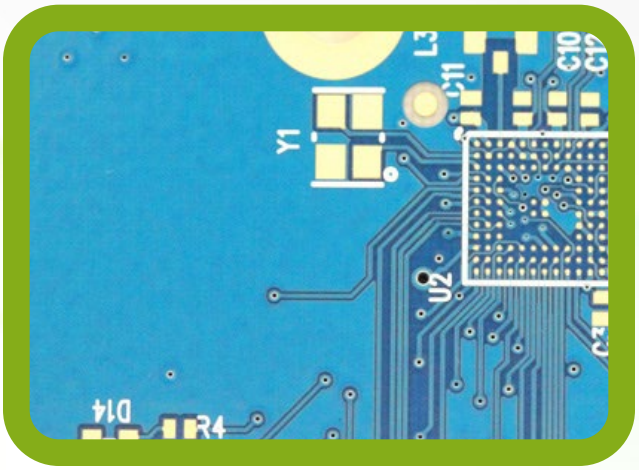

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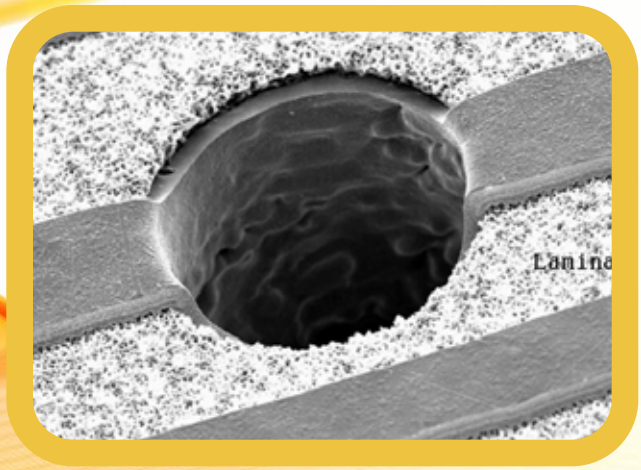

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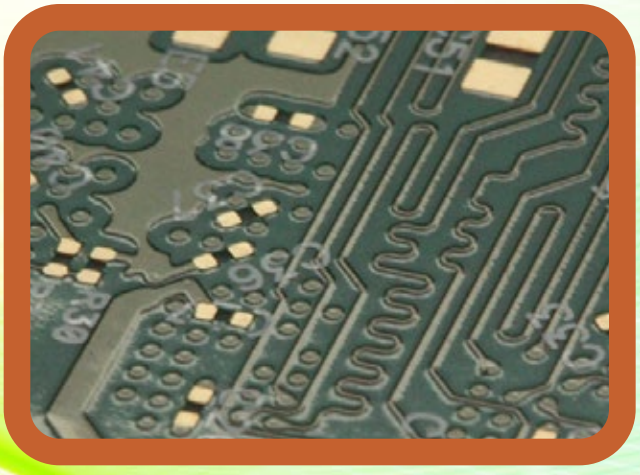

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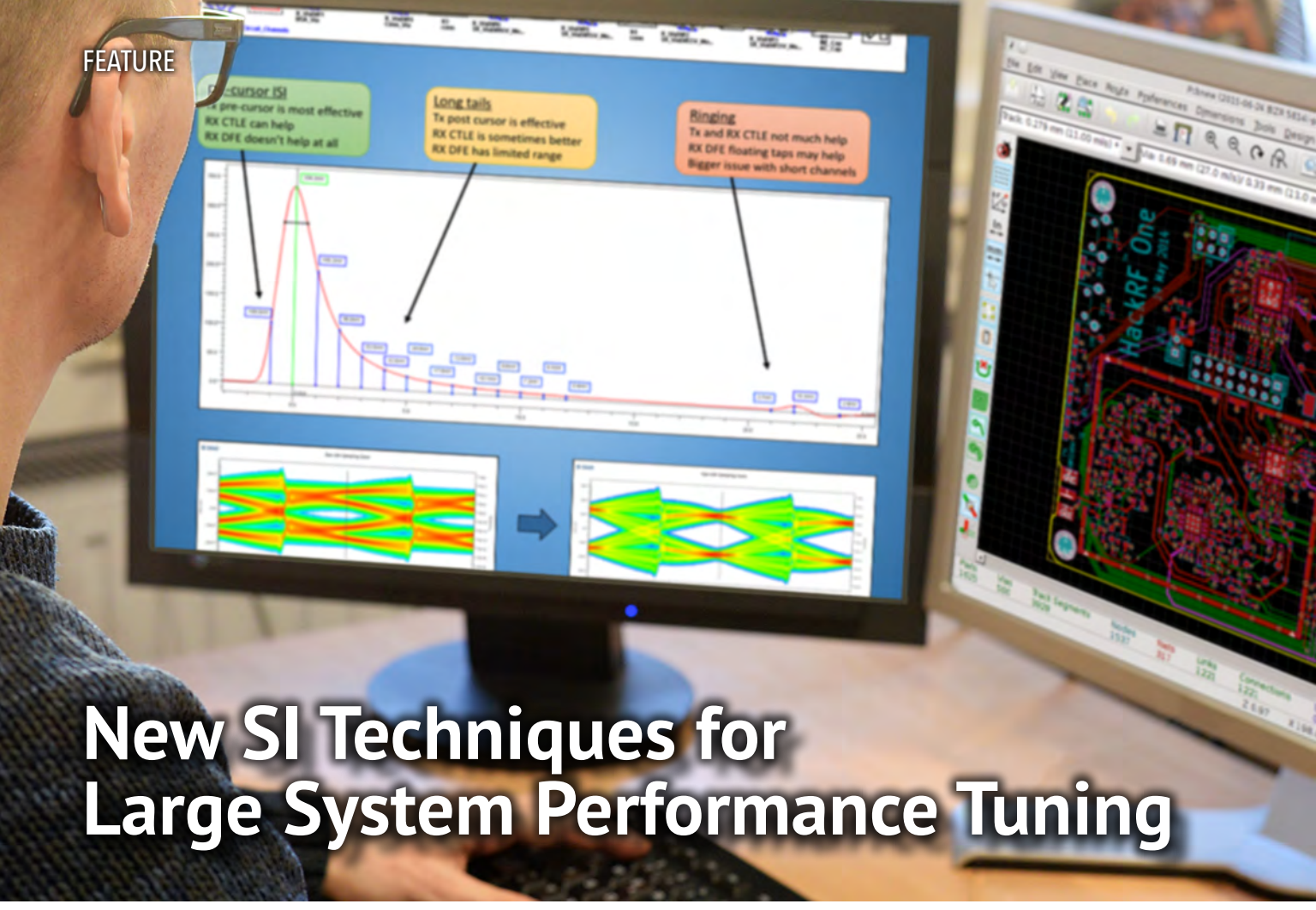

New SI Techniques for Large System Performance Tuning

by Donald Telian, SIGUYS,
and Michael Steinberger, Barry Katz, SISOFT

This paper was originally published in the proceedings of DesignCon 2016.

Abstract

Large systems with multiple configuration options and extended product lifecycles provide performance tuning opportunities such as SerDes setting optimizations and manufacturing improvements. This paper describes newly-developed techniques for equalization tuning and discontinuity reduction, offering additional design margin. Cost reductions are also achieved as new signal integrity (SI) techniques demonstrate performance parity removing non-essential re-timers and PCBs layers. This is the fourth in a series of DesignCon papers detailing the design and implementation of a system characterized by multiple thousands of interconnected serial links spanning dozens PCBs, operating at 3rd and 4th generation serial link data rates (6 to 12 Gbps).

1. Introduction

Simulation advancements released over ten years ago [1,2,3] allowed examination of serial links in greater detail, identifying performance limiters [4, 5] which motivated further refinements in the same [6]. Once tuned, the technologies were scaled to rapidly scan thousands of serial links to identify failure modes in rogue channels [7] enabling their correction and confident transition into production using simulated bit error ratios (BERs) as a qualifying metric [8]. This paper leverages and enhances these same technologies to provide large-system SerDes setting optimization and cost reduction, highlighting recent advancements in equalization optimization techniques and algorithms.

SerDes setting optimizations are applied to a wide range of channels across systems of various sizes. Optimization techniques are described, automated, applied to thousands of links and performance gains are quantified. SerDes tuning processes were simpler when one or two taps were available in the Tx and the Rx equalization options were few. However, with

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newer technologies the number of setting options grows exponentially as a larger number of Tx taps are available and trade-offs must be made between Tx and Rx equalization. As such, new tuning techniques are necessary. Furthermore, using re-timers to handle excessively long channels (40+ inches) seemed essential in previous generations of serial links. However as PCB and SerDes technologies continue to improve—combined with the optimization techniques described—we find that re-timers may not necessarily warrant their associated cost, complexity, and real estate.

Manufacturing improvements that enhance performance are also described. One example of a short connection with seven discontinuities spread across multiple PCB layers that initially showed multiple impedance changes in the 25% range is demonstrated to become nearly transparent over time. Relentless measurements on bare PCB fabrications, good vendor communication, and manufacturing process improvements and controls are key. Breakout traces longer than ¼" should be compensated. However, intentional trace layout manipulation in the presence of impedance control and re-imaging during fabrication must be carefully managed. Dual-diameter via construction is shown to be a viable solution for reducing discontinuities when via lengths exceeds 200 mils, by using simulation confirmed by lab measurement to achieve 20% channel eye improvement in channels of various lengths. SI analysis also verifies acceptable performance in reduced layer-count PCBs to achieve lower cost.

This is the fourth in a series of DesignCon papers from the authors, detailing the signal integrity analyses associated with a very large system design. The system is characterized by 7,000+ square inches of circuit board, multiple thousands of interconnected serial links spanning dozens PCBs, operating at 3rd and 4th generation serial link data rates (6 to 12 Gbps).

2. Performance Tuning Using SerDes Setting Optimization

This section illustrates system-level SerDes setting optimization performance tuning examples across large, medium, and small systems. For each system, baseline "coded" SerDes settings will be contrasted with "optimized" settings, where "coded" settings represent the previously best-known configuration for the SerDes based on previous simulation and hardware testing [4,7,8]. In other words, "coded" represents the settings coded into the system before optimized settings were derived.

The system configuration examined required PCBs with newer SerDes technology to interoperate with PCBs using older SerDes technology, as shown in Figure 1. The system integration scenarios involved various connectors and modularity, not shown in Figure 1 for simplicity. As newer SerDes (red, at right) can compensate for additional loss, their PCBs typi-

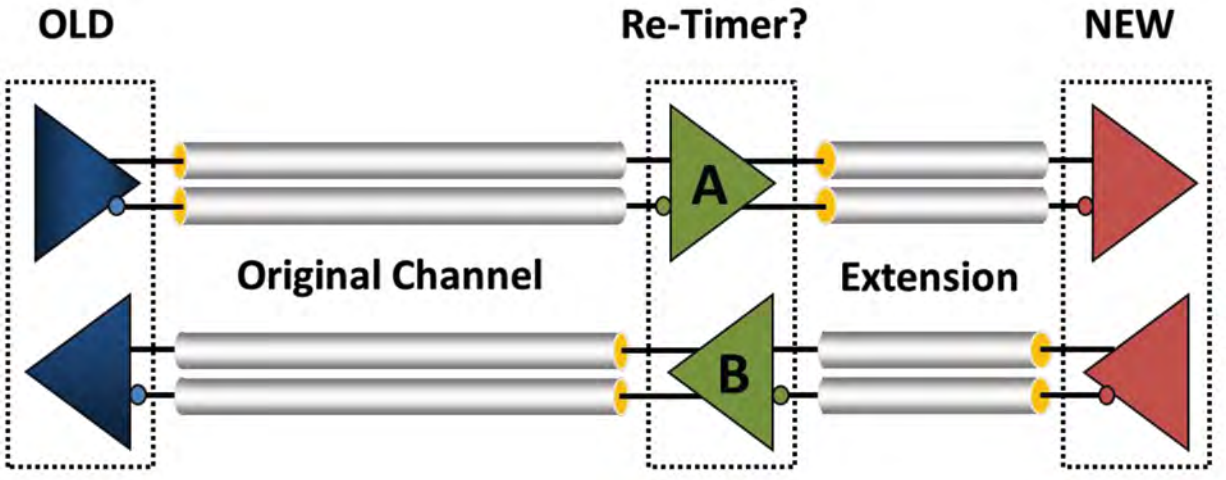

Figure 1: System configuration combining serdes generations.

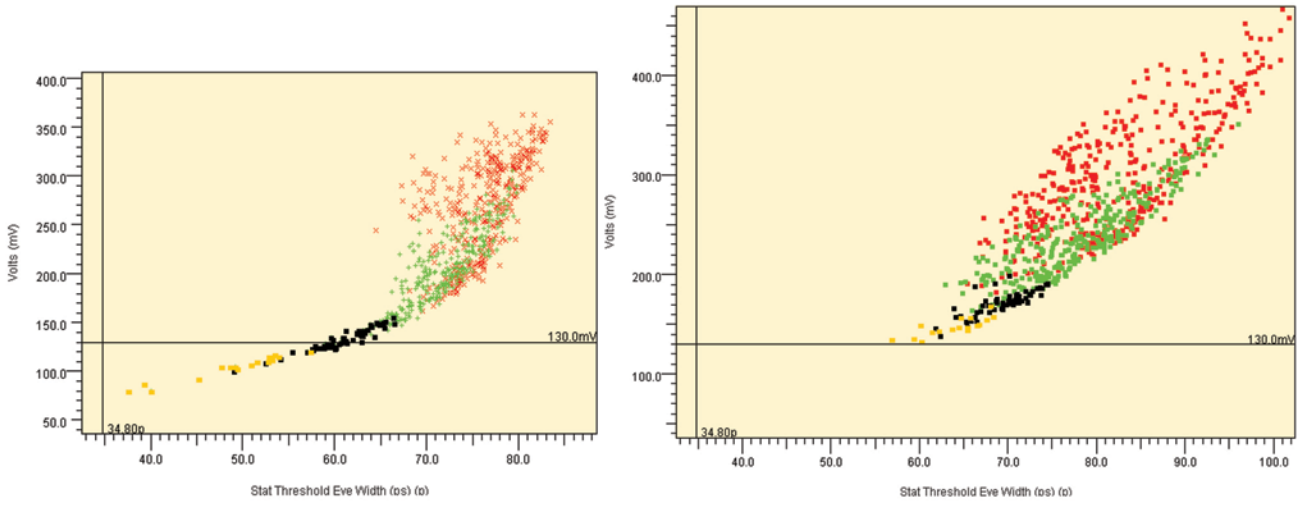

Figure 2: Simulated results, best-known settings (left), optimized settings (right).

cally include additional route length, marked in Figure 1 as an "Extension" to the "Original Channel" at left. This additional length raises the question of the need for re-timers (green, at center) when combined with older SerDes (blue, at left).

While the Tx in newer SerDes adds some new features, more significant changes have been made in Rx technology as CTLE (continuous time linear equalization) and DFE (decision feedback equalization) implementations continue to improve. As a result, it can be shown that the upper signal path in Figure 1 (old Tx driving new Rx) functions acceptably with the additional route length rendering the re-timers unnecessary in position "A." More challenging is the lower signal path (new Tx driving old Rx), thus reducing the design problem to assessing the need for the re-timer in position "B."

Since older technology is involved, real-time auto-negotiation of Tx settings in the physical system is not an option and other forms of channel optimization must be found. A design-time methodology, more fully described in the next section of this paper, is utilized to derive optimal performance given the available configurations and setting options in the SerDes involved. Specifically, the design task is to determine if the FFE (feed forward equalization) taps in the newer Tx can present an acceptable signal to the older Rx without the use of the re-timer in position "B." This analysis is performed using the system model previously described in [7,8].

The first, and most challenging scenario examined was the largest system which included thousands of serial links interconnected across dozens of PCBs. The plot at left in Figure 2 shows simulated eye heights and widths for ~1,000 channels implemented without a re-timer in position "B" versus design targets (horizontal and vertical markers). For this analysis, the channels were "coded" with best-known SerDes configuration settings. As shown, channels without the "extension" (red) perform acceptably against the targets, while some channels with the extension (green, with highlights in gold and black) are failing. Highlighted channels (gold and black) below and near the eye height target are those with the lengths up to 25% longer than initial budgets. Failures of such a linear nature are typically related to additional length and loss.

To address the failing channels, an initial implementation of channel optimization algorithms was tested with the results shown at right in Figure 2 (same color schemes). As shown, the performance of all channels exceeds design targets with more than 60% improvement in eye height and width for the worst-case channels. Performance comparisons revealed improvement in more than 85% of channels using these initial optimizations, motivating further refinements in the algorithms. Most importantly, Tx

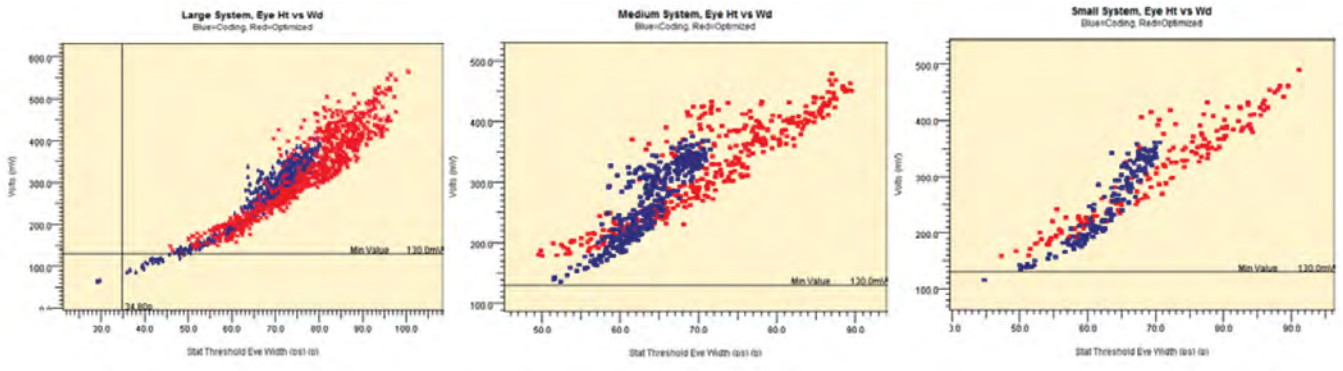

Figure 3: Default vs optimal eye openings for large, medium, and small systems.

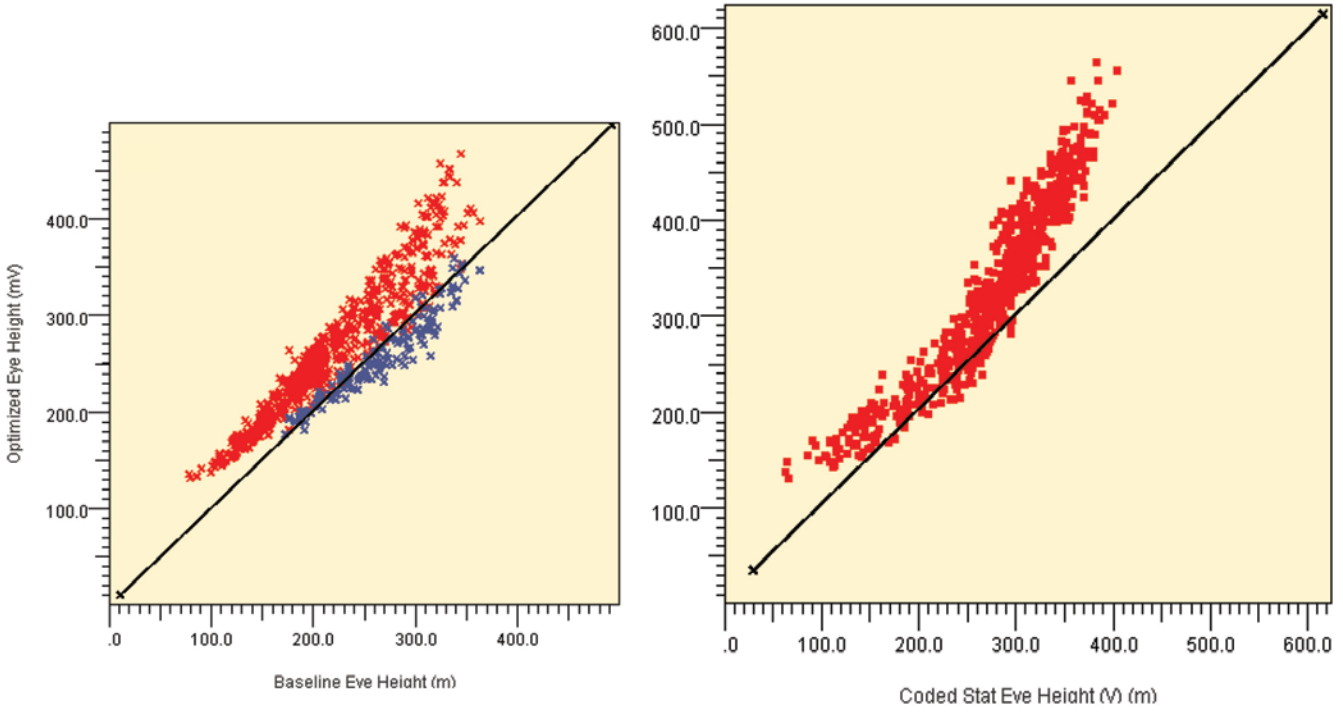

Figure 4: Eye heights contrasted, original (left) and improved (right) optimization algorithms.

settings had been derived that moved channel performance within design targets for the worst-case channels (gold and black). The axes in Figure 2 are aligned for easier comparison.

As similar PCB/SerDes combinations were deployed in systems of differing scale, performance was examined for all scenarios. The plots in Figure 3 compare the eye openings using default SerDes coding (blue) against optimized coding (red) for three system sizes: large (left), medium (center) and small (right). These simulations add additional system-level jitter and improved optimization algorithms, and illustrate how optimization moves worst case channels within design targets (lower left corner, all plots) while providing improved margin for all channels.

For the largest system, Figure 4 shows optimization improvement by contrasting simulated eye heights using both the original algorithm (left) and the improved algorithm (right). Each point in the plots represents one channel. For each channel, the X axis plots simulated eye height using the original (baseline) SerDes cod-

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ing and the Y axis plots the eye height derived from the optimized coding. As such, points on the diagonal black line represent channels that performed the same using either SerDes configuration. Channels above the line have better eye heights using optimization, while points below the line represent channels with better eye heights using the baseline coding. The plots show that the optimized settings exceed the baseline in 85% of the channels using the original algorithm (left) and 95% of channels using the improved algorithm (right). As desired, worst-case channels in the lower-left corners of both plots increasingly move away from the black line. The Y axes are aligned to show ~100mV gain in some channels.

In both cases in Figure 4, the default (non-optimized) coding is better in some mid-range channels. The channels highlighted in blue (left) represent channels that did not trade tap one optimally between the Tx and Rx in the original algorithm, as this trade-off is not simple to derive. Although the optimization techniques described in the next section will detail the removal of intersymbol interference (ISI) by forcing the pulse response to zero in pre- and post-tap UIs, in some cases that method does not provide the optimal result. In Figure 5, the zeroforcing solution (blue) produces a smaller eye than the one derived by the refined automated algorithm (red). In some cases the complete elimination of ISI can remove too much amplitude from the main cursor (compare red and blue at ~8.25 nS). As such, optimization algorithms must intelligently trade-off amplitude, Tx/Rx taps, equalizable ISI, residual ISI in long tails, and other factors to arrive at the optimal solution. This is not a simple task—particularly since the "optimal" solution may vary depending on performance criterion.

3. System-Level Channel Optimization Techniques

3.1 Overview

One of the tasks to be performed in the analyses shown in the preceding section was to optimize the combination of transmit and receive equalization separately for each channel in the system. Given the number of channels to be optimized, an automated procedure was required.

The optimization procedure we used is based on an analysis of the impulse response at the output of the receiver's IBIS-AMI model. The procedure is based on a pulse response derived from the impulse response and assumes

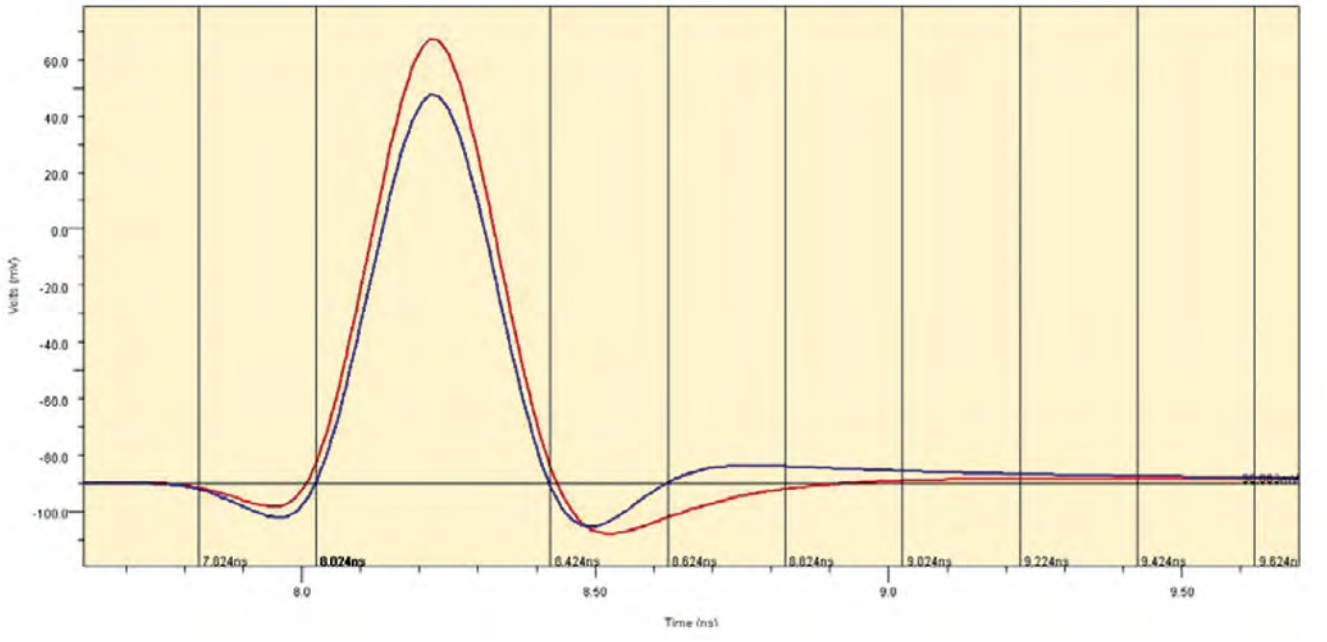

Figure 5: Pulse responses derived using conceptual and automated techniques.

that there are three equalization mechanisms applied to the channel:

1. Transmitter feed-forward equalization (FFE).
– The FFE is assumed to be a synchronously spaced tapped delay line with linear taps, in which the equalizing taps can occur either before or after the main tap.
– It is assumed that the maximum transmit voltage is constant, which is achieved by keeping the transmit swing constant and the sum of the absolute values of the taps equal to one.
2. Receiver continuous time linear equalization (CTLE).
– The CTLE is assumed to have a finite number of configurations which can be chosen through the IBIS-AMI model's input parameter string.
– No assumption is made concerning the relationship of one CTLE configuration to another.
3. Receiver decision feedback equalization (DFE).
– The DFE is assumed to be a synchronously spaced tapped delay line with linear taps, driven by the detected data.
– It is assumed that the detected data is almost always correct.

The overall procedure is

1. Define a starting configuration for the transmitter and receiver.
2. Solve for the impulse response of the passive interconnect network.
3. Apply the transmitter IBIS-AMI model to the channel impulse response, resulting in an impulse response at the input of the receiver model.
4. For each CTLE configuration:
a. Set the receiver IBIS-AMI model to the selected CTLE configuration and apply the receiver model to the input impulse response.
b. Using Hilbert space projection, compute the combination of FFE and DFE taps that will minimize the intersymbol interference.
c. Using Banach space techniques, adjust the FFE and DFE taps to maximize the eye height.
d. Record the best eye height, CTLE configuration, FFE and DFE tap values.
5. Set the FFE taps in the transmitter IBIS-AMI model to the selected tap values and set the receiver IBIS-AMI model to the selected CTLE configuration. It is assumed that the receiver's DFE will perform its own adaptation.
6. If the FFE tap values have changed significantly since the last time they were set, go back to step 3 and repeat the optimization algorithm. If the FFE tap values have not changed significantly, execute the statistical analysis in the normal manner.

The procedure described was first implemented in a simplified form in 2002. While the initial approach was reasonably successful, the subsequent evolution has made the procedure much more complex and introduced a number of subtle details. These details, and the optimal automation of the same, are beyond the scope of this paper.

This paper will instead present techniques that system developers can apply manually to a pulse response in a waveform viewer either to obtain an equalization configuration that is close to optimum or to gain insight into the trade-offs that the optimization must address. The emphasis is on insight rather than automation.

The manual procedures to be described in subsequent sections are

• Clock recovery: The optimization procedure is critically dependent on the position of the recovered clock. An algorithm we call the "hula-hoop" algorithm quickly and accurately determines the average clock timing to be expected from a bang-bang clock recovery loop.

• Minimize intersymbol interference: Choose FFE and DFE tap weights that will minimize intersymbol interference, and understand how these choices will affect the eye height.

• Maximize eye height: Understand how minimizing the intersymbol interference improves eye height but does not obtain exactly the maximum eye height.

• CTLE vs. FFE trade-offs: The effect of CTLE can be very similar to the effect of FFE, often

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making the two mechanisms almost interchangeable. The low frequency gain of a given CTLE configuration determines how desirable that configuration is compared to a similar result obtained using FFE.

• FFE vs. DFE trade-offs: In some ways, the effect of DFE can be very similar to the effect of FFE; however, there are also some important differences that affect the way the two mechanisms should be used together.

3.2 Clock Recovery

An examination of the threshold crossing time distribution due to intersymbol interference for a number of different examples led to the conclusion that these threshold crossing time distributions are always symmetrical, or nearly so. This makes sense in that the effect of an intersymbol interference contributor on the transition time of a data edge is reasonably close to linear. That is, if a given intersymbol interference contributor delays the data transition by a specific amount when the interfering bit is a "one," then the data transition will be advanced by almost exactly the same amount when the interfering bit is a "zero."

Therefore the effect of all the interfering bits balances out (or nearly so) and both the median and mean transition times are determined by the primary transition from a "zero" in the preceding bit to a "one" in the bit to be detected, and back to a "zero" in the bit following the bit to be detected. In other words, the recovered clock timing will be half way between the transition times for a 010 data pattern in isolation.

Equivalently, we can examine the pulse response, looking for two non-zero values which are exactly one bit time apart and equal to each other. The recovered clock will be half way between those two samples. We call this algorithm the "hula hoop" algorithm because if one imagines the pulse response to be a solid object (such as a length of bent wire) and one were to drop a ring with one UI diameter (the "hula hoop") on that object and level it, the center of the ring would be at the recovered clock time.

Figure 6 illustrates the procedure as applied in a waveform viewer. This procedure only takes a minute or two, and is quite precise.

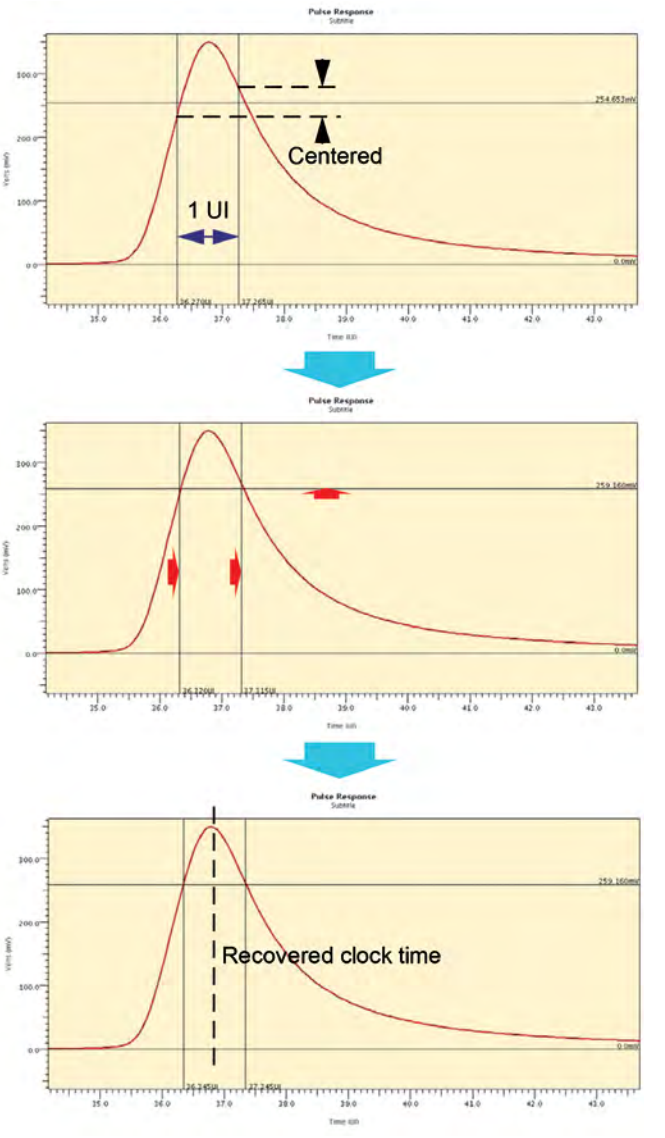

Figure 6: Hula hoop algorithm as implemented in a waveform viewer.

1. The user starts by placing two vertical markers exactly one UI apart in a position that straddles the main pulse.

2. The user places a horizontal marker that is centered between the points where the vertical markers intersect the pulse response.

3. The user shifts both vertical markers to approximately the intersection of the horizontal marker with the pulse response, while keeping them exactly one UI apart.

4. Steps 2 and 3 are repeated until both the vertical markers and horizontal marker inter-

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sect the pulse response while the vertical markers have remained one UI apart.

5. The recovered clock time is half way between the two vertical markers. This recovered clock time and times before and after that are an integer number of UI away are the times at which the intersymbol interference is to be evaluated.

3.3 Minimizing Intersymbol Interference

Given the recovered clock time, the next step is to choose FFE tap weights that minimize the intersymbol interference. Note that changing the FFE tap weights can affect the recovered clock time; so given the FFE tap weights that minimize intersymbol interference, it may be desirable to recover the clock time again and then fine tune the FFE tap weights. Figure 7 shows the same pulse response as in Figure 6, indicating voltage samples that are spaced an integer number of UI apart. The desired sample is V[0] and the remaining samples are intersymbol interference.

Since in a real data signal the adjacent bits can be either "zero" or "one," it's the absolute values of the intersymbol interference samples that matters. Assuming that the data signal is a balanced NRZ signal, the corresponding signal voltages are -0.5 and +0.5. The minimum eye height is then

$$V_{min} = V[0] - \sum_{i \neq 0} |V[i]| \qquad \text{(EQ1)}$$

One of the most important characteristics of FFE is that the effect of an individual tap persists much longer than the time at which the tap was applied. Thus, when applying the manual procedure, it's important to apply the earlier FFE taps before the later ones because each tap affects the impact of subsequent taps.

In the current example, the first tap is a single precursor tap. We will therefore determine its tap weight before addressing the postcursor taps. Suppose that the tap weight for the precursor tap is W[-1] and the tap weight for the main tap is W[0]. We have assumed that the sum of the absolute values of all the taps is one. Furthermore, we are assuming that the main tap is positive, and we can observe that the precursor tap is going to be negative. Therefore the tap weight constraint is

$$-W[-1] + W[0] = 1 \qquad \text{(EQ2)}$$

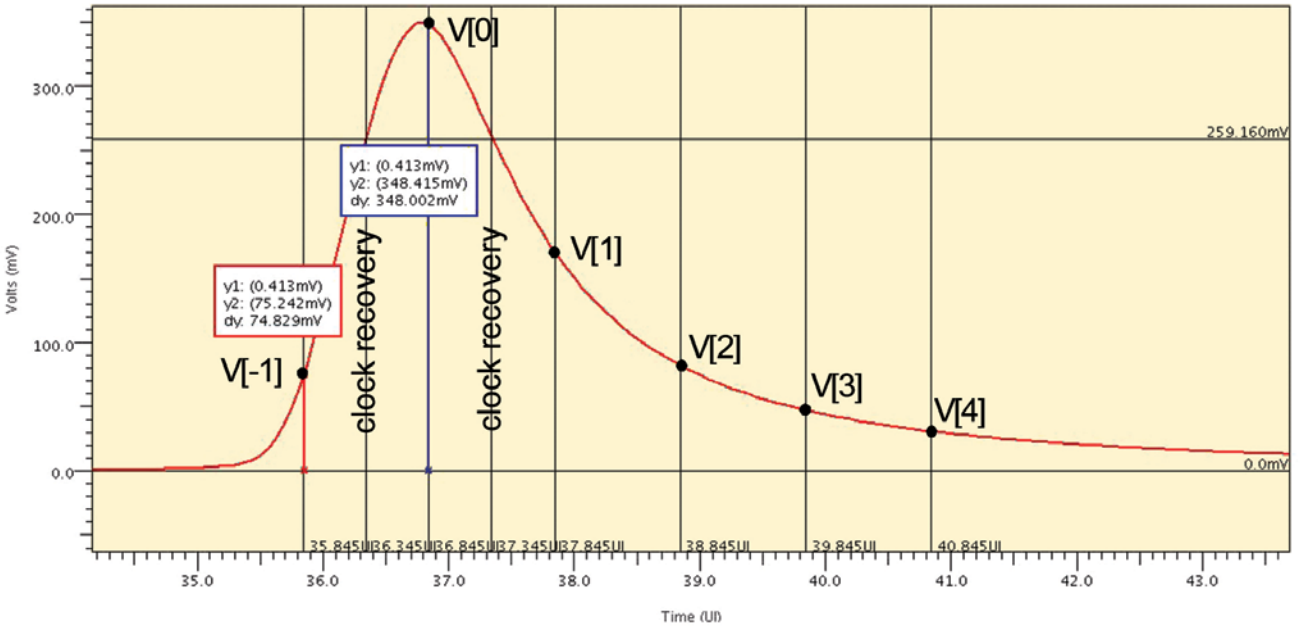

Figure 7: Intersymbol interference samples.

We also desire that the precursor tap should zero out the intersymbol interference at the precursor position. In other words, the signal contribution from the precursor tap at the precursor tap time (W[-1]V[0]) should cancel out the signal contribution from the main tap at the precursor tap time (W[0]V[-1]). Still keeping in mind that the main tap will be adjusting the amplitude of the main pulse, the desired condition is

$$W[0]V[-1] + W[-1]V[0] = 0 \qquad \text{(EQ3)}$$

Solving these ewo equations,

$$W[-1] = -\frac{V[-1]}{V[-1] + V[0]} \qquad \text{(EQ4)}$$

$$W[0] = \frac{V[0]}{V[-1] + V[0]} \qquad \text{(EQ5)}$$

Applying these equations to the values shown in Figure 7 produces the result shown in Figure 8. Note in Figure 8 that when the precursor tap response (in green) modifies the original pulse response (in red), the resulting pulse response (in blue) goes through zero at the precursor tap position. Note also that the amplitude of the main pulse has been reduced significantly, and that there was some equalization at the postcursor tap positions.

The calculation of subsequent tap weights follows the same process; however, the equations become much more difficult to solve algebraically. Note the voltage V'[1] measured at the first postcursor bit position in Figure 8. For the first postcursor tap, the equations are

$$W[-1] \approx -\frac{V[-1]}{V[-1] + V[0] + V'[1]} \qquad \text{(EQ6)}$$

$$W[0] \approx \frac{V[0]}{V[-1] + V[0] + V'[1]} \qquad \text{(EQ7)}$$

$$W[1] \approx -\frac{V'[1]}{V[-1] + V[0] + V'[1]} \qquad \text{(EQ8)}$$

and the resulting pulse response is shown in Figure 9.

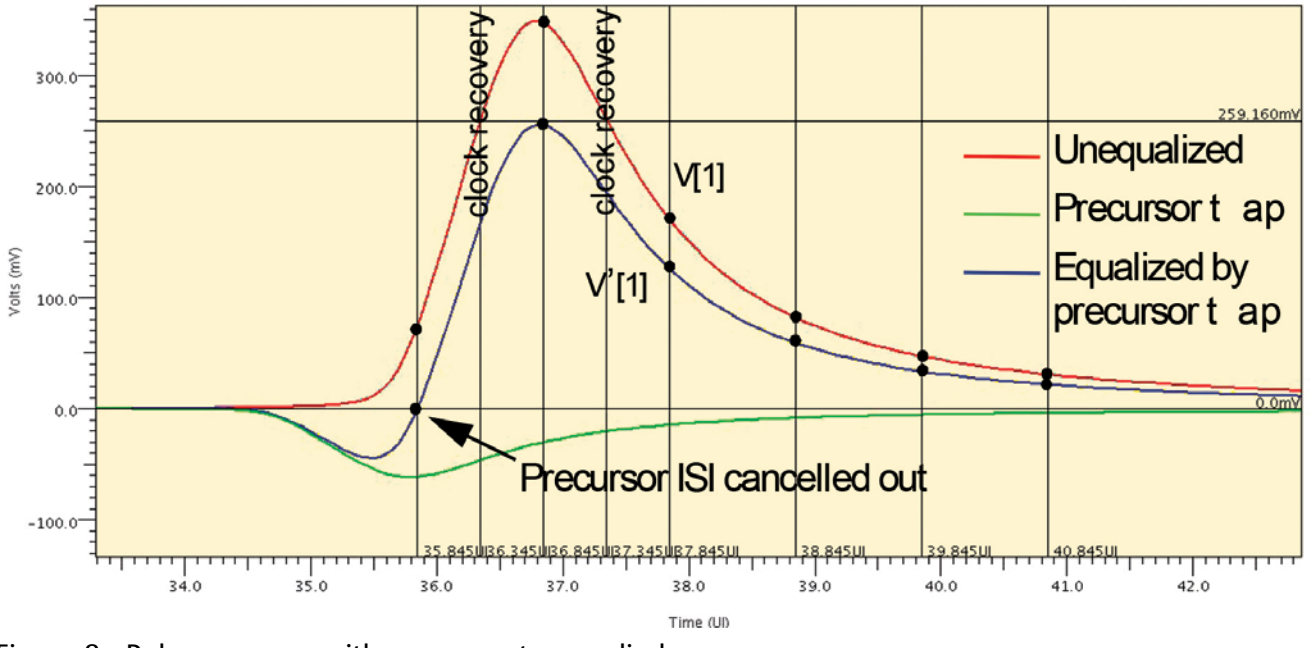

Figure 8: Pulse response with precursor tap applied.

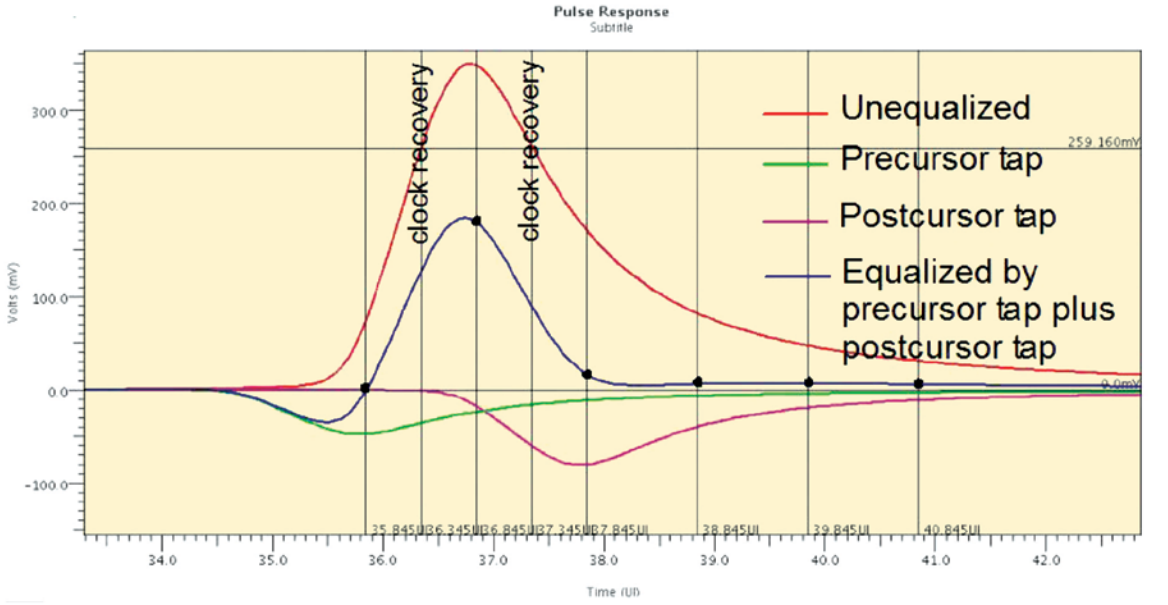

Figure 9: Pulse response equalized by precursor tap plus postcursor tap.

Several observations can be made from Figure 9:

1. One could improve the equalization solution by increasing the magnitude of the postcursor tap by a little bit. Note that when doing so, the other two taps would have to be adjusted as well, both to maintain tap weight normalization and to maintain good equalization at the precursor tap position.

2. The amplitude of the main pulse has been reduced by approximately a factor of two. This is one of the factors to consider when choosing FFE taps: equalization costs amplitude, reducing the energy delivered to the receiver.

3. The intersymbol interference at later symbols has been all but eliminated. This is especially true for a well behaved pulse response as shown in this example; however, the same phenomenon occurs for less well behaved pulse responses. In general, one FFE tap affects the intersymbol interference at multiple bit positions.

Equation 1 states that the minimum eye height is the main pulse response amplitude minus the sum of all the intersymbol interference amplitudes. FFE derives its effectiveness from the fact that even though it reduces the main pulse amplitude, it also reduces the intersymbol interference amplitude at many positions, thus gaining leverage from the amplitude that was invested in equalization.

The general form of Equation 6 through Equation 8 can be applied to estimate additional tap weights. However, for best results those tap weights should be adjusted manually after the equations have been used to provide the initial estimate. The overall procedure can be completed in less than an hour—practical for a few test cases but not for equalizing thousands of channels in a system.

3.4 Intersymbol Interference vs. Eye Height

While minimizing intersymbol interference goes a long way toward improving channel performance, intersymbol interference as a performance measure is not the same as eye height or eye width. Furthermore, the optimum configuration for one performance measure will probably not be exactly the optimum for another performance measure. Rather, the optimum configuration will be a function of the performance measure that was chosen. This section will concentrate on eye height because it's almost always harder to maximize than eye width.

In the case of the FFE tap weight calculations described above, the weight given to the equalizing taps subtracts from the main pulse, and therefore subtracts from the eye height. Therefore backing off slightly from the tap weights

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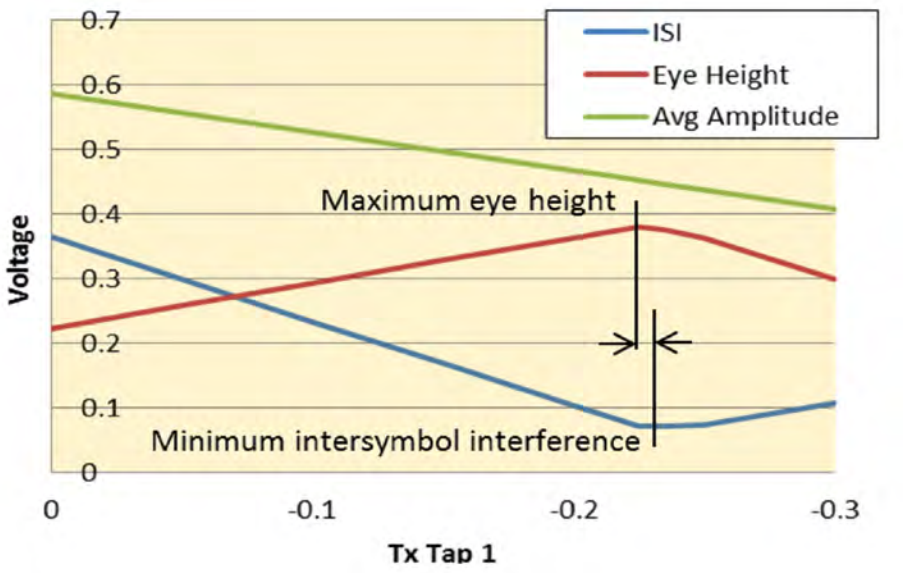

Figure 10: Trade-off between intersymbol interference and eye height for a single tap FFE.

for minimum intersymbol interference typically yields a slightly greater eye height.

Figure 10 is an example of the trade-off that can be expected for the case of a single tap FFE and a channel that is relatively easy to equalize. The green line is the average amplitude in the eye diagram at the receiver decision point, which is proportional to the main tap weight. The blue curve is the maximum intersymbol interference at the recovered clock time and the red curve is the minimum eye height at the recovered clock time. The red curve is equal to the green curve minus the blue curve (i.e., the average amplitude minus the intersymbol interference). In this case, reducing Tap 1 by a little over 4% increases the eye height by a little over 1%.

While more sophisticated algorithms are possible, for manual optimization it should be sufficient to reduce all of the equalizing tap weights in the FFE by a fixed percentage and add that amplitude to the main tap. It would be practical to evaluate the eye height for several different values of the fixed percentage; however, in most cases a value from 0% for channels that are difficult to equalize to about 5% for channels that are easy to equalize should be about right. **PCBDESIGN**

Due to the length of this article, we have published the remainder on the PCBDesign007 site. Click here.

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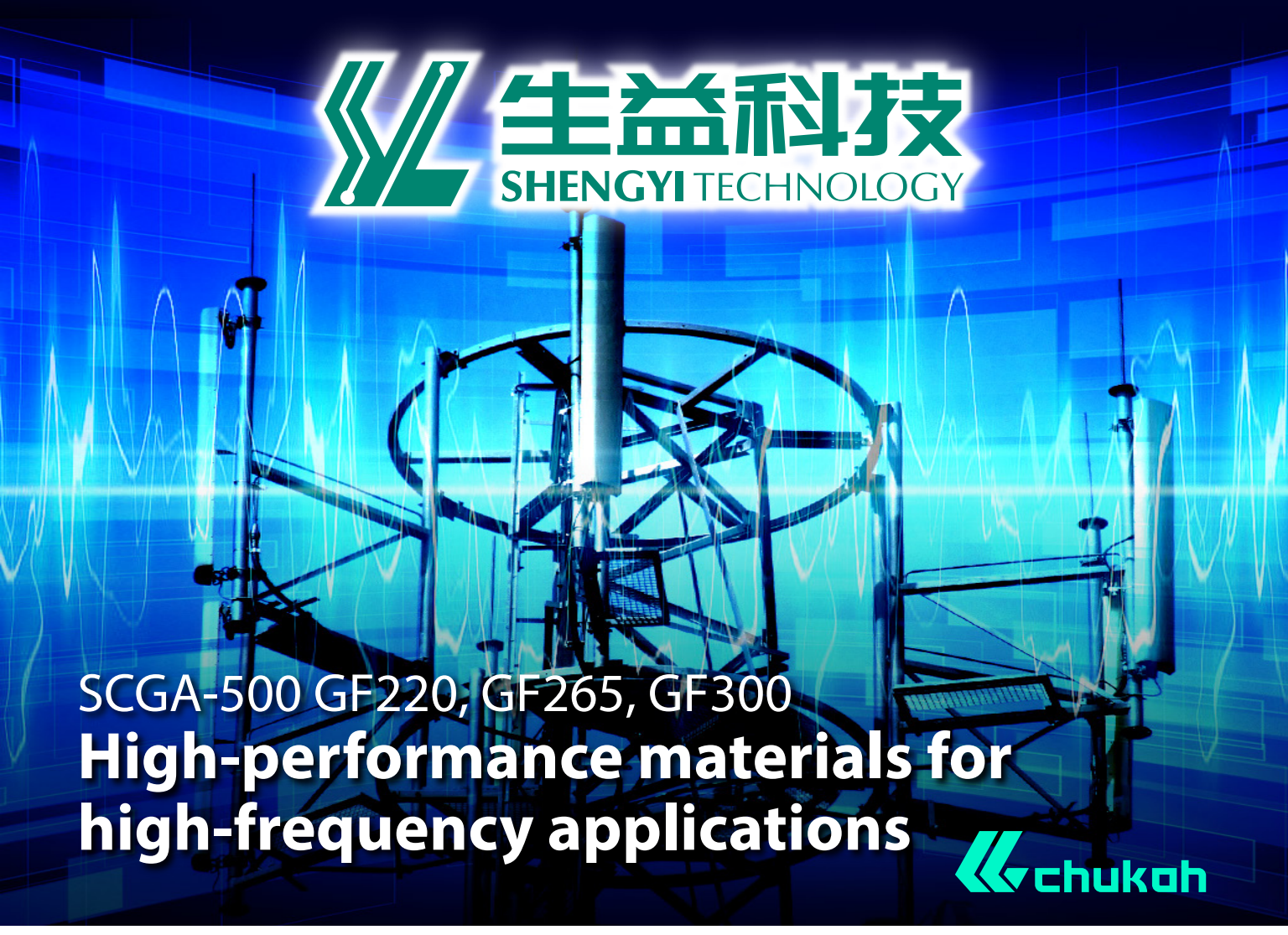
Michael Steinberger, Ph.D., lead architect for SiSoft, has over 30 years of experience designing very high-speed electronic circuits. He is currently responsible for the architecture of SiSoft's Quantum Channel Designer tool for high speed serial channel analysis. To contact him, click here.

Barry Katz, president and CTO of SiSoft, founded the company in 1995. As CTO, Barry is responsible for leading the definition and development of SiSoft's products. He has devoted much of his efforts at SiSoft to delivering a comprehensive design methodology, software tools, and expert consulting to solve the problems faced by designers of leading edge high-speed systems. To contact him, click here.



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SIGNAL INTEGRITY
Tools and Design Methodology in the Modern Age

by Dennis Nagle
CADENCE DESIGN SYSTEMS

The PCB design process has traditionally been done in silos. One group creates the design intent (schematic), another group implements the logic on the PCB, and yet another group does some checking of the design using analysis tools. This traditional approach has run into a number of problems.

The first problem was that prototypes were showing up in the lab that did not work due to complicated signal and power integrity problems not found by the analysis tools. But even when the analysis team equipped themselves with sophisticated analysis tools, the back-and-forth between silos or lack of time in the schedule tended to create chaos as design deadlines loomed.

Today, modern PCB design methodology offers a more team-oriented solution. With a front-to-back constraint driven approach that enables all groups to get involved with signal and power integrity, many potential problems are either avoided or found early in the design process. With first order problems removed, the analysis team, with their sophisticated tools, is better positioned to focus on design sign-off so prototypes come back working the first time.

This article is focused on how each part of that design team can get out of their silo and work cooperatively. Using a common constraint manager, each group can utilize their varying levels of expertise to ferret out signal and power integrity problems.

Pre-Layout

For teams seeking to break out of their historic silos, tools can help by providing a certain amount of integration. One way that can happen is by having a constraint system integrated with your SI system at all stages of your design process. While decisions are being made for physical partitioning, component/IP selections, and power requirements, pre-layout analysis can help define your solution space and corresponding electrical constraints. This early analysis as part of a well-executed constraint driven flow saves time and prevents issues from propagating down to SI signoff.

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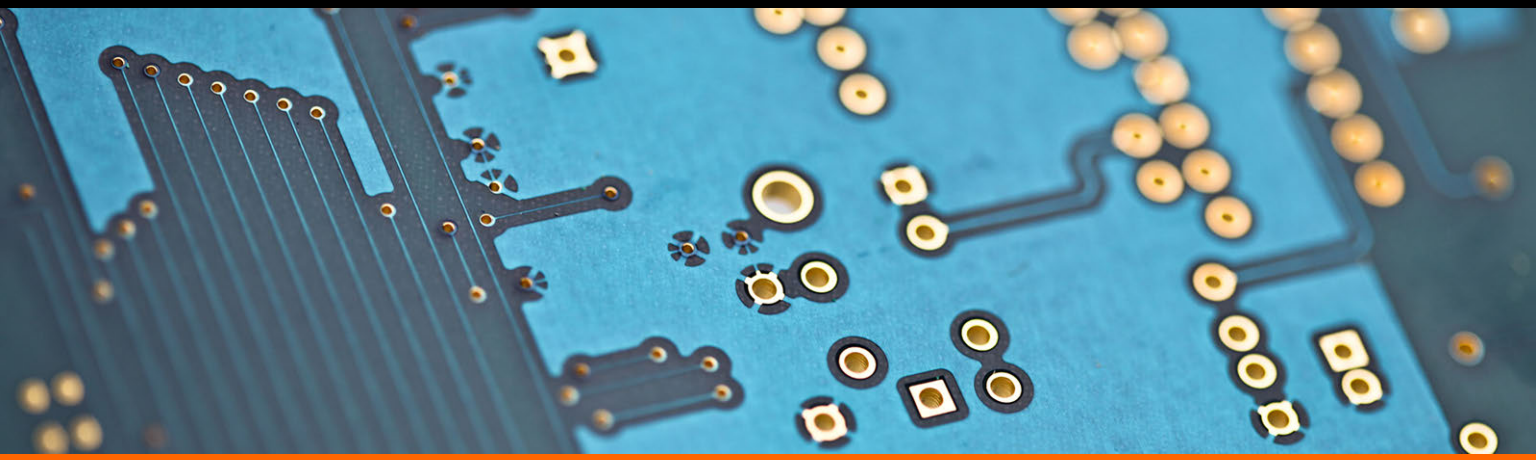

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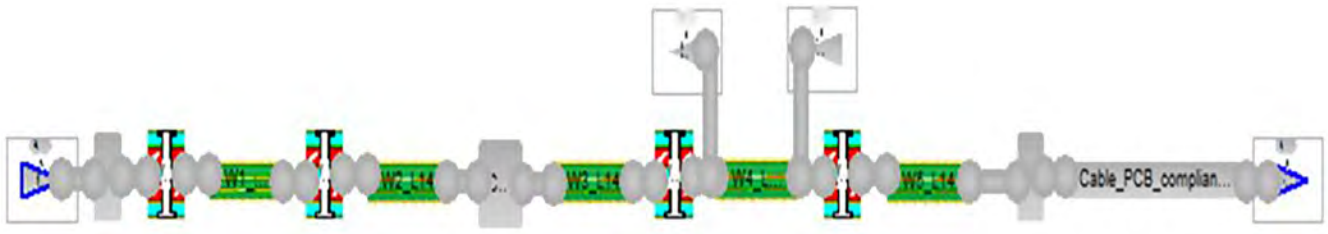

Figure 1: Pre-layout topology, with W-element and via models representing PCB interconnect.

Topology analysis is usually what comes to mind when thinking of pre-layout analysis and is an ideal environment for what-if analysis. Here you can start from scratch or by extracting nets from design data in the schematic or layout. In either case you can quickly build a representation of the major interfaces in the design. Models for active devices should be as accurate as possible and interconnect can be estimated or parameterized and swept.

Topologies that can be extracted from schematic and layout can allow all team members to access the same data for scheduling or constraint purposes. This can also enable design engineers to address reflection and topology issues along with the SI engineer. The topology can be used to drive scheduling of the nets for routing and placement and capture any other relevant constraints.

While a topology may be the first thing that comes to mind when thinking of pre-layout analysis, an often overlooked capability is that of virtual prototyping. This can be used to address situations where a netlist or design database isn't available when an SI engineer would like to create a specific prototype. Ideally, this would leverage existing design and library data for PCB layout such as stack-up, padstack, and footprints. These virtual prototypes can provide additional insight into placement and routing for simulations and constraint development that would not be possible with a topology. It is never expected to be a full representation of the design and can be extremely helpful in evaluating specific interfaces.

Whether topology or virtual prototype, both should be supported by structured device model management. Your SI models should get the same attention as schematic symbols and layout footprints. Analysis model management promotes reuse and saves setup time. Pre-layout analysis will identify cases where new models are needed which can then be validated and promoted to the central library. Even better is a process where the central library management system is fully integrated to include analysis models. This allows model assignments in the library data to track SI models as the design progresses from schematic to layout. Topology extraction from these design databases should support passing device models to the topologies.

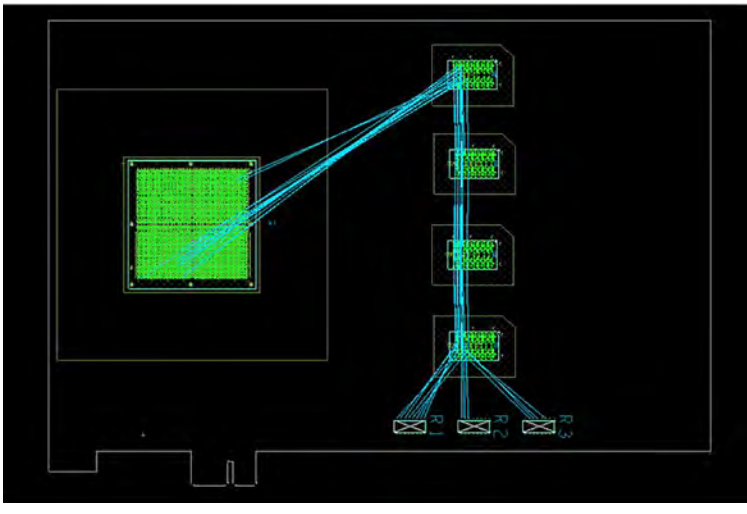

Figure 2: Virtual prototype of DDR3 interface with scheduling applied to address bus.

Floorplanning

While pre-layout analysis represents a starting point, floorplanning is where the actual physical layout starts to take shape. Pre-netlist floorplanning is where placement and form factor or other mechanical/thermal requirements are examined. But floorplanning should con-

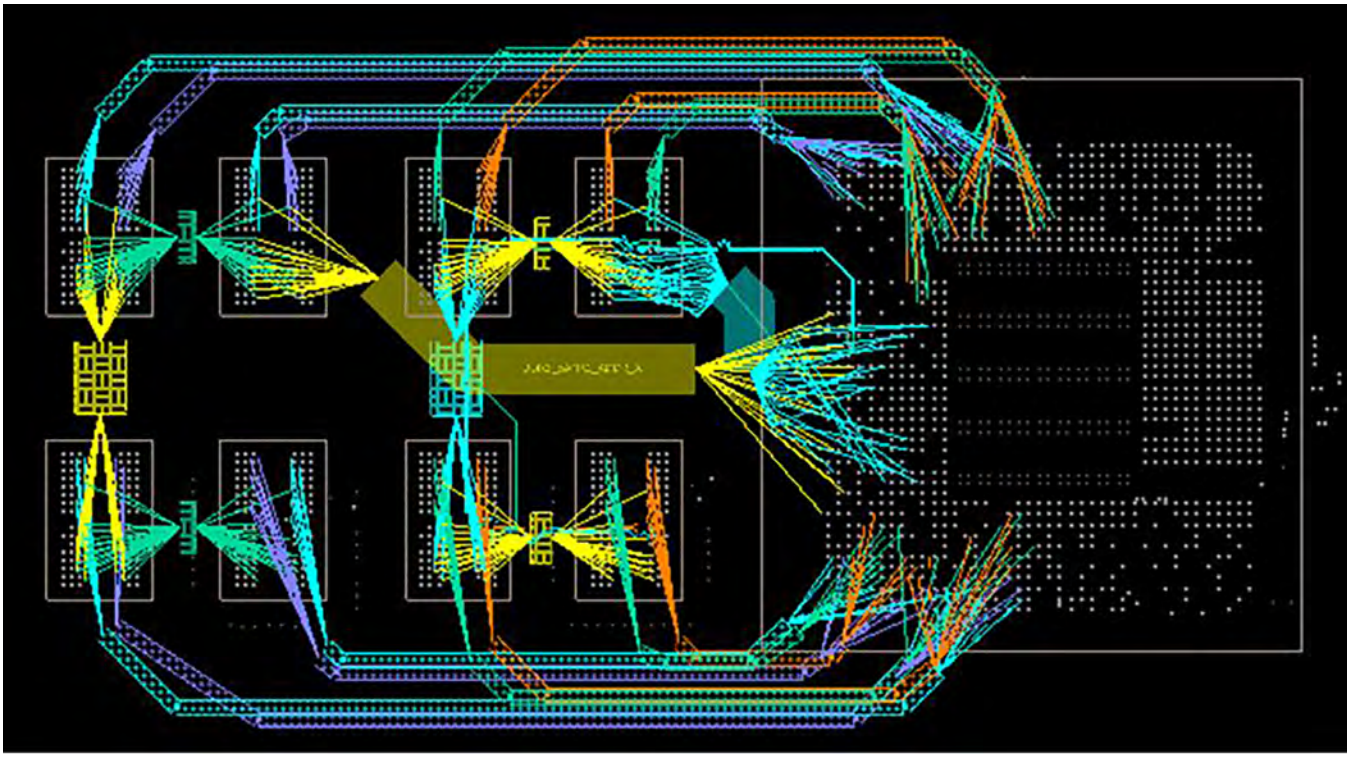

Figure 3: Example of a design with nets represented in bundles to guide routing.

tinue once a netlist is ready and loaded into a layout-based application. This is really where design specific SI analysis can and should start even before any routing.

Why? There's an obvious goal of reducing the overall effort required for SI signoff and there's plenty that can be analyzed prior to the routing even starting. Let's take a look at what we typically concern ourselves with in the SI domain. We have signal quality with challenges like overshoot and ringback, timing-related issues like delay, what kind of routing topology works best for the situation and whether or not termination is needed, and of course crosstalk. The only one of these that absolutely requires routed traces in place is crosstalk.

This represents an ideal time to simulate the entire design, and in particular the interfaces that were not captured and simulated with topologies, for any of those SI issues, with the exception of crosstalk. Device model data assignments have propagated to the layout database as part of the netlist and simulating with unrouted nets will be quick since the interconnect is represented with a simple ideal model based on Manhattan distance and an impedance. In some cases, the Manhattan distance can be replaced with design data to give a more accurate estimate of how certain nets will be routed. This can be useful at the pre-route stage to improve the accuracy of SI analysis.

Floorplanning stage analysis can lead you to placement edits or changes which are too painful after investing any time in routing. This is another example of where the constraint system and SI analysis leveraging the same design data can improve the overall process.

Screening

At this stage of the design, the focus is rule checking. Constraints and rule checking will drive any automated or manual routing with DRC violation feedback from the rules developed and implemented in the earlier stages. This traditional constraint-driven design methodology was born roughly two decades ago. Over the same time, data rates have gone from tens of Mbps to several Gbps for parallel interfaces plus we've seen the dawn of serial interfaces with even higher data rates. As a result,

DRCs now share the screening limelight with ERCs (electrical rule checks) and SRCs (simulated rule checks). As these names imply, they involve more than just traditional physical rule checks and rely on some of the same data we use for traditional SI analysis.

This represents an ideal time for the layout designer to catch as many potential SI issues before any post-layout analysis. Impedance and coupling can be checked and resolved without the need for any complicated setup or analysis. Results can be more than simple violation markers to provide better visual clues to violations and areas that need attention.

The most critical thing to consider for today's designs is how power and signal interaction affects signal integrity. As the design progresses and PDN structures such as planes are implemented, coupling among power nets, signals, and vias can and should be evaluated. Many constraints are formed at the early stages of a design before planes and vias exist. Performing physical rule checking as these elements are added should not be based on the assumption of ideal planes. Impedance, trace coupling, crosstalk, delay, and skew need to account for the impact of power noise upon signals.

This new breed of SRCs performs analysis of signal and power coupling by applying a linear excitation to large number of signal nets. These SRCs report signal quality including all coupling noise while avoiding any time consuming non-linear simulation. The results guide layout designers to find issues general post-route rule checking, assuming ideal reference planes, cannot find. One example of this is where via coupling from a plane can induce crosstalk that increases as the traces are separated. This seems to violate not only common sense but also any traditional crosstalk rule that relies on ideal reference planes. It can only be captured when plane noise and via coupling are considered.

At this stage the device models assigned in the layout may not get exercised for each type of DRC, ERC, or SRC but it can be very advantageous if the same analysis engines and accurate solvers used for SI analysis can be accessed by the rule checking. We will examine some of these advanced engines in the next section.

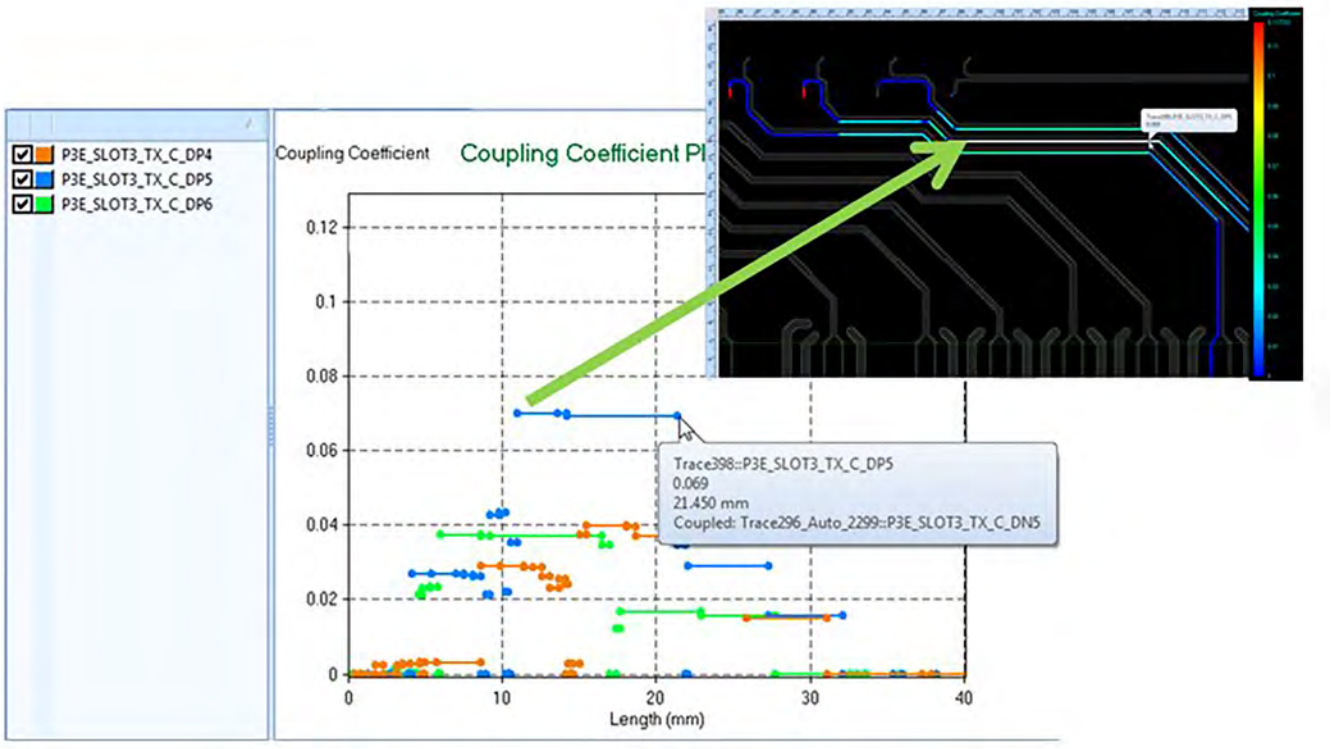

Figure 4: Overlays and plots can provide better visualization of constraint issues.

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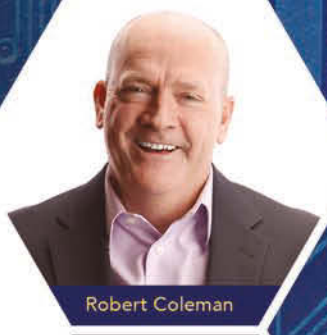
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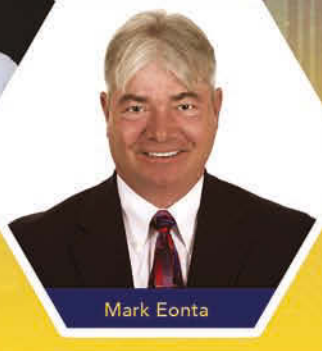
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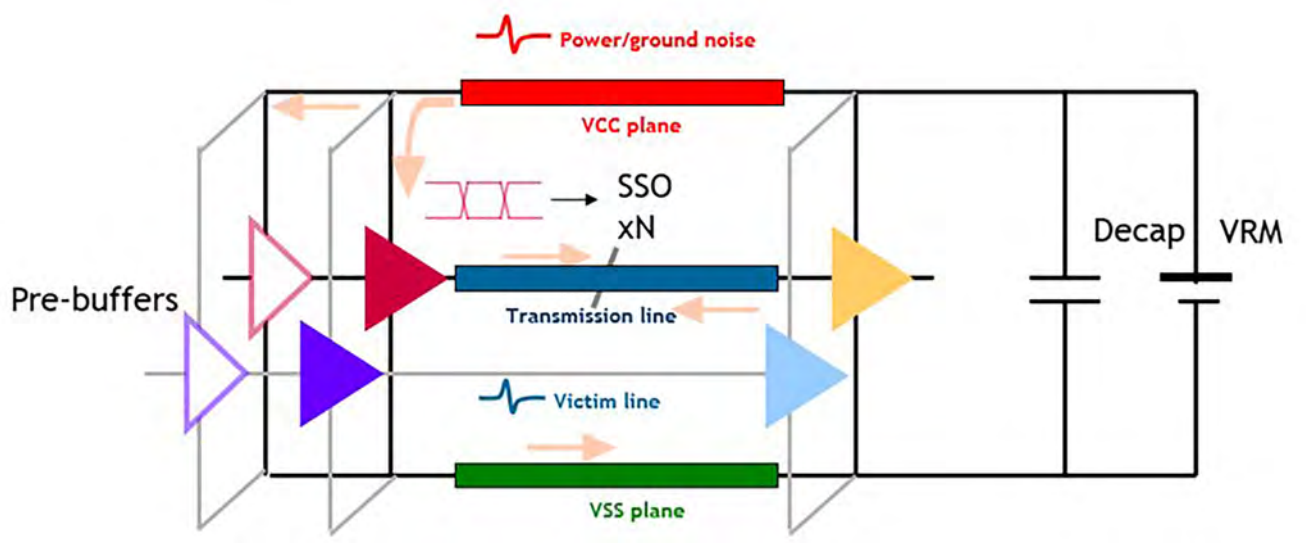


Figure 5: An SSN simulation.

Detailed Simulation

With the board-level screening passes completed, the design DRC-clean, and no significant reflection or crosstalk issues remaining, it is time to focus on the final stage of analysis. This typically involves detailed simulation to perform compliance analysis for the multi-gigabit interfaces in the design. These will commonly be DDR memory and serial link interfaces, with protocol-specific criteria to be evaluated.

Assuming analysis began in the pre-layout stage, this largely consists of performing detailed interconnect extraction of layout, replacing the "postulated" pre-layout W-element and via models with extracted S-parameters, and re-running simulation/compliance checking for final design margins.

For today's DDR interfaces, the power distribution network (PDN) needs to be extracted along with the signals, to account for non-ideal power effects, such as simultaneous switching noise (SSN).

The most practical way to do this today is with a "hybrid" electromagnetic (EM) solver, which decomposes copper structures into vias, transmission lines, and shapes, solves them with application-specific solvers, and recombines the overall result into an S-parameter model. Including non-ideal power effects into DDR simulations prevents potential problems from being masked by ideal plane assumptions.

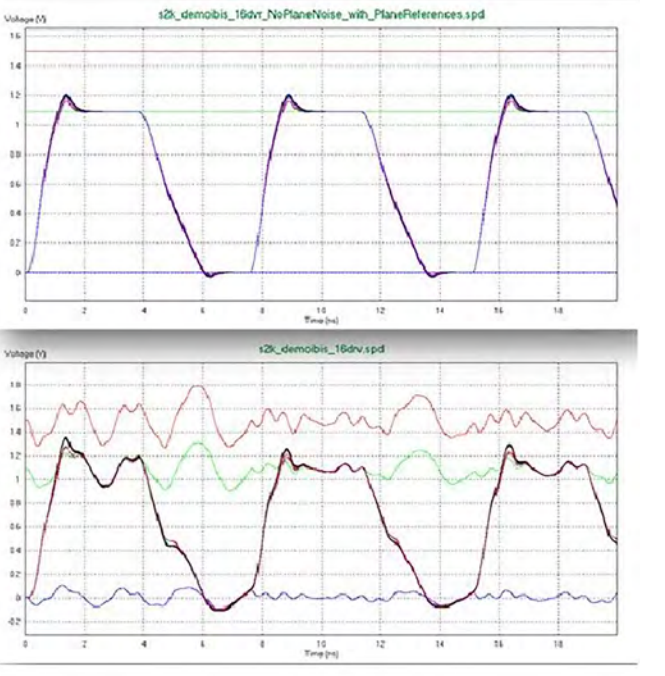


Figure 6: Signals assuming ideal power (top) vs. non-ideal power (bottom).

The extraction for high data-rate serial link interfaces must also be done with care and requires even high levels of accuracy. While uniform PCB traces can be modeled nicely with today's 2D field solvers, the via arrays used for layer transitions will usually require full wave 3D extraction for accurate representation.

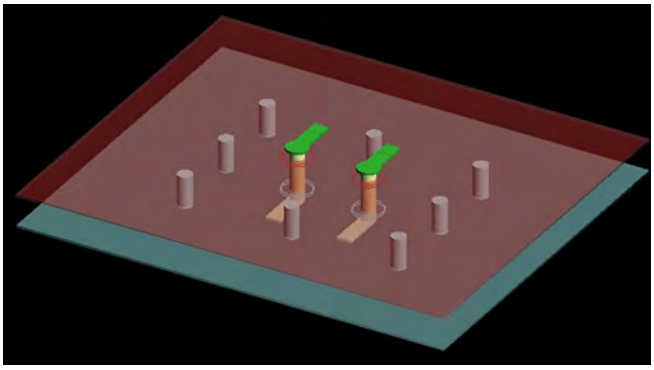


Figure 7: 3D via array structure.

Those layer transitions often create the largest impedance discontinuities seen in the signal path, and play a key role in the accuracy of the overall channel model.

Full-wave 3D solutions are computationally intensive, and it can easily take several hours to extract a set of differential pairs coupled together. The 3D meshing done along the long uniform PCB traces is a significant culprit in the overall solution time, and is unnecessary for these largely 2D structures. A "cut-and-stitch" methodology can be used to focus the more expensive 3D field solution where it is warranted, while traditional 2D techniques can be used to quickly solve uniform transmission lines. This "full wave where you need it" approach, combining multiple field solvers, can be automated by cutting out the serial link path from the overall design, breaking it up into "cutting zones," and designating those zones for the solver of choice. The project can be automatically broken down, solved in pieces, and re-combined into a composite S-parameter.

With accurate S-parameter extraction completed, pre-layout test benches can quickly be updated, incorporating the detailed interconnect models into the analysis.

Similar attention needs to be paid to device modeling. Multi-gigabit interfaces generally utilize equalization to achieve the required signal quality. Interfaces running over 10Gbps usually use adaptive equalization techniques, where the equalization behavior changes over a period of time. Traditional time step-based circuit simulation cannot run enough data traffic in order for the equalization to adapt, produce enough samples in the eye distribution, and enable bit error ratio (BER) to be extrapolated. These types of interfaces require channel simulation, which uses impulse response techniques to simulate high-capacity traffic. Channel simulation also enables IBIS-AMI device models to be used. These types of device models incorporate exe-

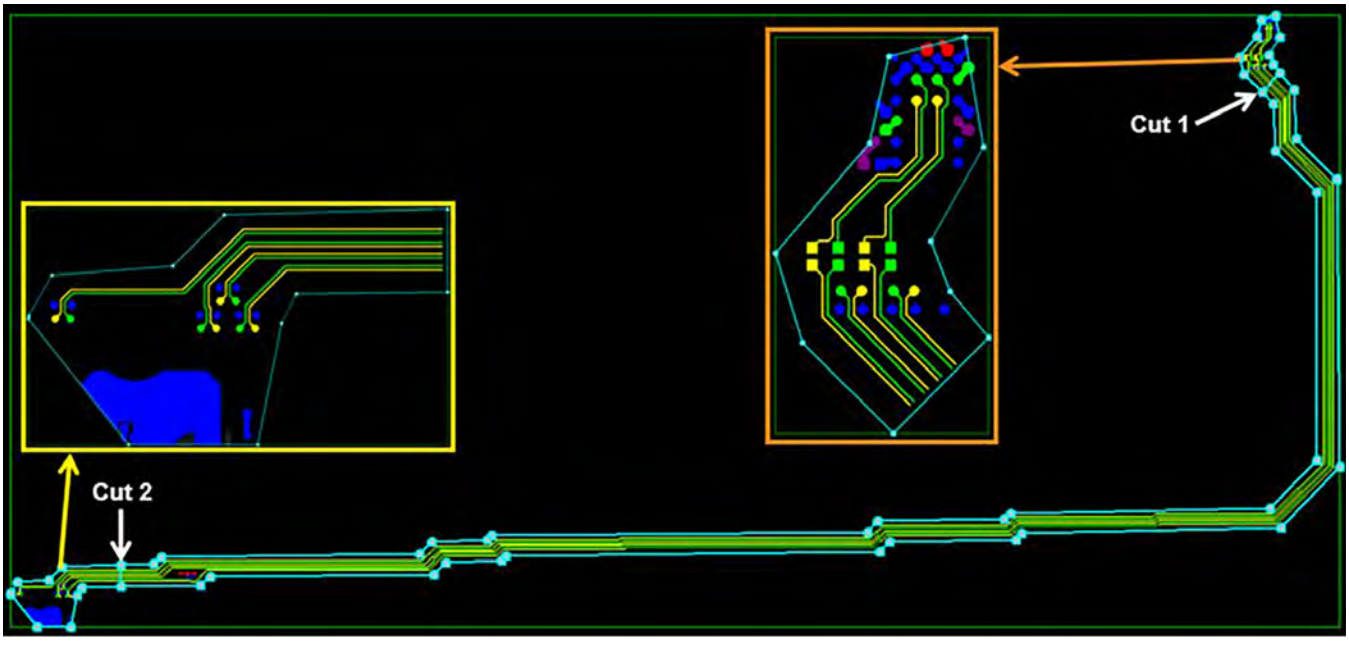


Figure 8: Cut and stitch approach.

cutable software modules, which can model the types of adaptive equalization commonly used today, such as continuous time linear equalization (CTLE), decision feedback equalization (DFE), and feed forward equalization (FFE).

While IBIS-AMI models are much more readily available for SerDes devices than just a few years ago, there may still be situations where an IBIS-AMI model is not available for a specific device, but you know the general characteristics of its equalization, such as the number of FFE taps or the CTLE frequency response. In these cases, today's tools enable you to quickly synthesize the IBIS-AMI model you need to carry out the simulation, and simulate your system-level interface.

With appropriate interconnect and device models in place, you can get down to the business of verifying compliance for your critical high speed interfaces. For DDR interfaces, the landscape is changing. Starting with DDR4, memory interfaces are starting to adopt serial link modeling and analysis techniques. Memory controllers now have the FFE and CTLE techniques that serial links have had for many years, and because of that, are beginning to use IBIS-AMI models as well. In addition to device modeling, we now see standards like DDR4 moving from a traditional setup and hold time compliance approach to a mask-based one, like those historically seen for serial links, along with specific BER requirements.

Checking compliance for signal quality and mask adherence for entire memory interfaces full of signals (and even multiple interfaces in

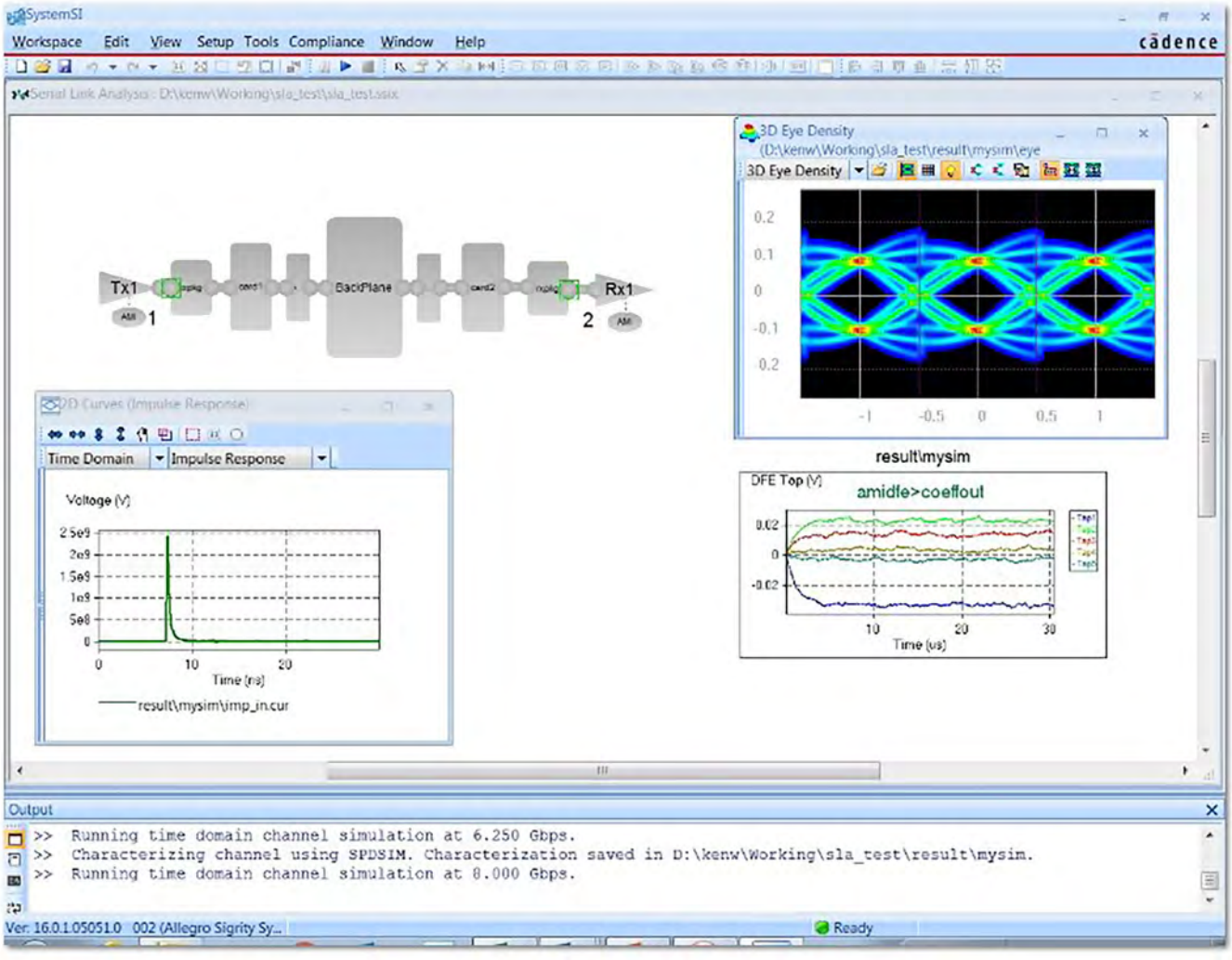


Figure 9: Serial link analysis including equalization from IBIS-AMI models.

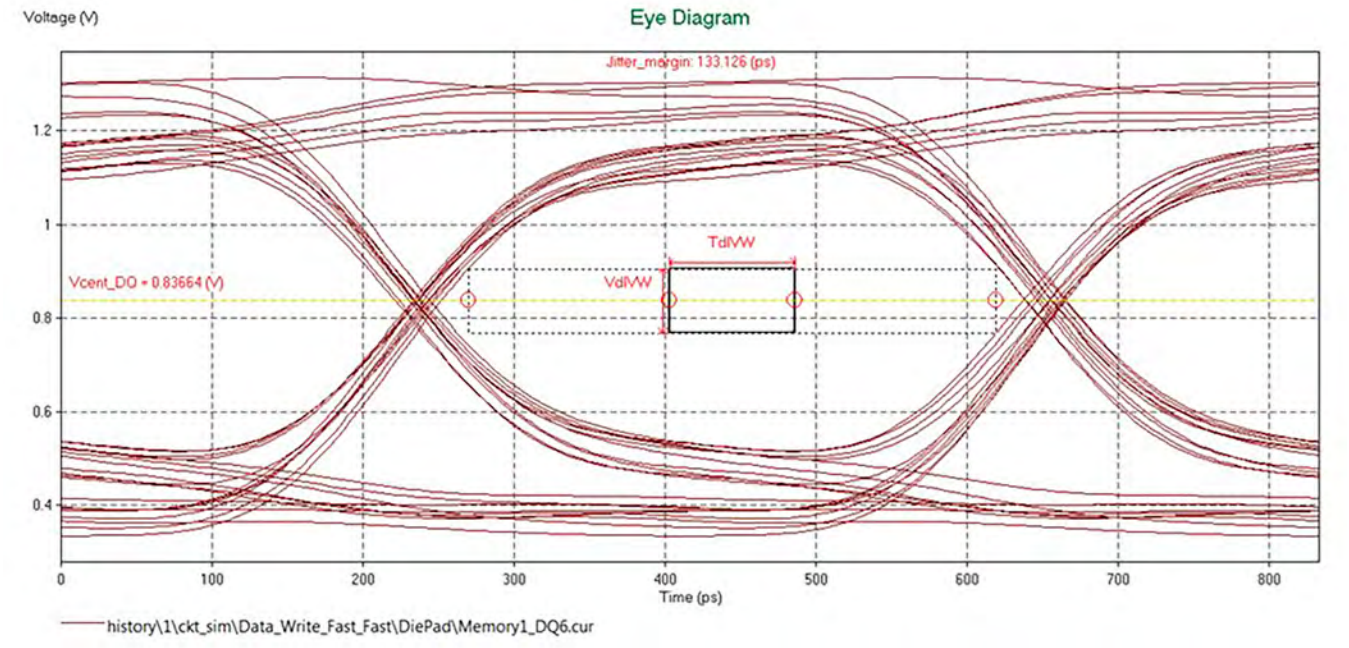


Figure 10: Mask-based compliance for DDR4 signals.

a design) can be very time-consuming, so good automation of waveform post-processing is essential, along with generation of detailed sign-off reports.

In addition to the mask-based compliance checking above, serial link compliance will often have other unique requirements for the interface, including specific frequency domain characteristics for the interconnect.

In summary, thorough verification flows from good pre-layout analysis. Simulation test benches used up front can be re-used and updated with detailed interconnect models extracted from layout. Different types of EM solvers are needed to perform power-aware bus extraction for DDR interfaces, and intelligent deployment of full-wave techniques is needed to efficiently characterize layer transitions for high data rate serial link interfaces. Automated, interface-specific compliance analysis needs to be applied to the final design, allowing you to sign off your design to fabrication with confidence, and help achieve first-pass success in the lab.

No.	Parameter	Symbol	☑
Channel Tolerancing Eye Mask Values (table 4-27 in PCI Express Base spec.)			
1	Eye Height	$V_{RX-CH-EH}$	☑
2	Eye Width at Zero Crossing	$T_{RX-CH-EW}$	☑
3	Peak EH Offset from UI Center	$T_{RX-DS-OFFSET}$	☑
4	Range for DFE d_1 Coefficient	$V_{RX-DFE-COEFF}$	☑
5	Eye Mask		☑
Differential Insertion Loss (figure 4-66 in PCI Express Base spec.)			
6	Insertion Loss	SDD21	☑
Differential Return Loss (figure 4-56 in PCI Express Base spec.)			
7	Tx Return Loss	RL - Tx	☑
8	Rx Return Loss	RL - Rx	☑
Stressed/Swept Jitter Test (figure 4-74 in PCI Express Base spec.)			
9	Stressed/Swept Jitter		☑

OK Cancel

Channel Tolerancing Eye Mask Values

Item	Value	Simulation Results		Pass/Fail
Eye Height	25 mV	$V_{RX-CH-EH}$ (mV)	68.572	Pass
Eye Width at Zero Crossing	0.3 UI	$T_{RX-CH-EW}$ (UI)	0.361	Pass
Peak EH Offset from UI Center	±0.1 UI	$T_{RX-DS-OFFSET}$ (UI)	0.062	Pass
Range for DFE d_1 Coefficient	±30 mV	$V_{RX-DFE-COEFF}$ (mV)	-0.006	Pass
Eye Mask		Eye Mask		Pass

Figure 11: PCI Express Gen 3 compliance criteria.

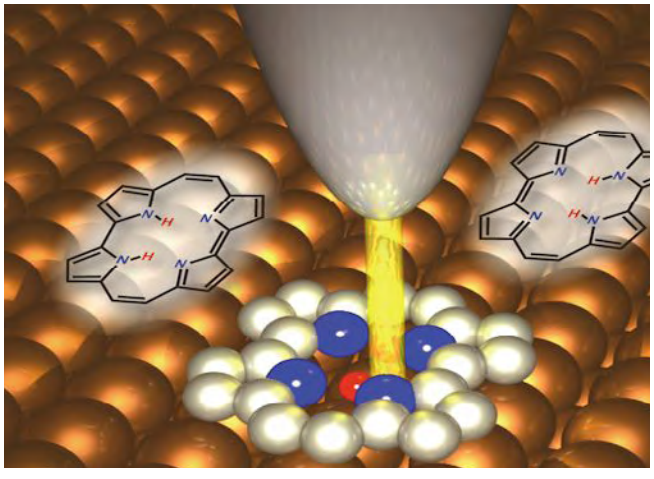
Conclusion

Design engineers can create constraints and plan out bus routing. PCB Designers can quickly screen a design for both physical and electrical rule violations. And signal and power integrity engineers can run detailed simulations that they can count on as being highly accurate. While this may not sound like a new concept, there is now integration of analysis technology in the design environment that enables all members of the team to use the same underlying analysis capabilities with varying levels of detail and expertise.

Utilizing common libraries, common constraints, and common analysis engines makes for a unique and highly communicative environment. No more silos! By enabling all members of the PCB design team to have a role in the electrical integrity of the design, fewer problems are found in the lab and fewer design iterations are required. This results in meeting time to market requirements and having a predictable schedule. **PCBDESIGN**

Dennis Nagle is a product engineering architect at Cadence Design Systems.

Chemists Show New Way to Operate a Single Molecular Switch



Researchers at the University of Liverpool are part of an international team that have shown a new way to operate a single molecular switch based on mechanochemistry.

In a study published in Nature Chemistry, the team which included Fritz-Haber Institute of the Max Planck Society (FHI-MPG), Berlin, Donostia International Physics Center, San Sebastian and the Polish Academy of Sciences, showed how hydrogen atoms in a single organic molecule adsorbed on a surface can be switched in a controlled manner on a sub-molecular scale by the force from an atomically sharp, metallic tip.

This so-called tautomerization of hydrogen atoms is an important reaction in organic chemistry and molecular biology and is also a promising process for realizing single-molecule switches in molecular device applications.

In addition, by using chemically modified tips, this tip-induced process also provides a new strategy to gain a deeper atomistic insight into catalytic reactions and a new control of single-molecule chemistry.

Liverpool Chemist Professor Mats Persson said: "This research is a new finding in the field of mechanochemistry and has implications for the development of future nanotechnologies in particular molecular devices such as switches for molecular electronics."

Takashi Kumagai at FHI-MPG, who initiated the study, wanted to explore the question of how much force is needed to operate a single-molecule switch. To address this, the researchers attached an organic molecule that exhibits tautomerization to a surface and approached the tip of a combined atomic force and scanning tunneling microscope within a few atomic distances above the molecule.

The research team also carried out extensive computer simulations in order to elucidate the atomistic mechanisms behind the force-induced tautomerization. Their calculations revealed that the tautomerization occurred by a reduction of its energy barrier upon approach of a metallic tip, while it could not be induced by a tip terminated by a Xe atom due to its inertness and softness.

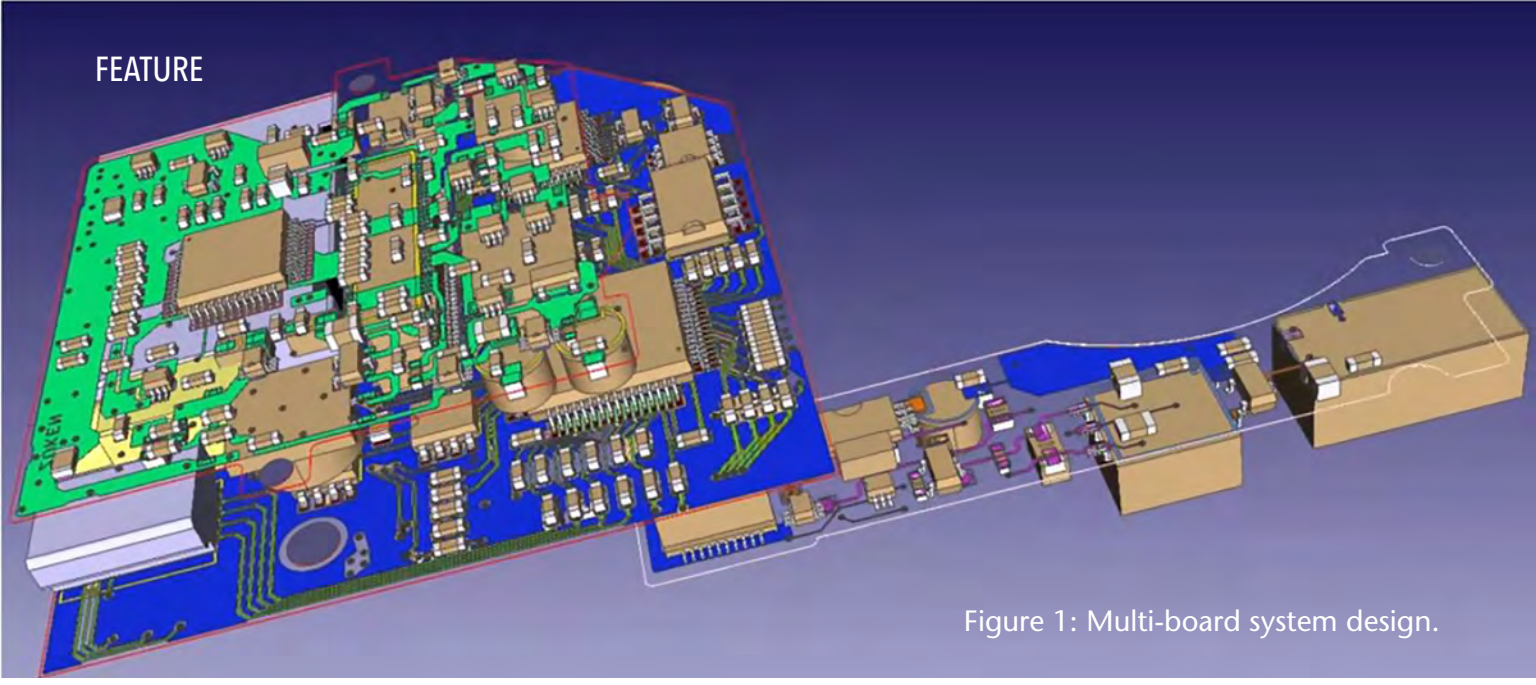


Figure 1: Multi-board system design.

Getting Signal Integrity Right by Design

by Narayanan TV
ZUKEN

As clock frequencies increase and active devices and interconnect traces shrink and are placed ever closer together, signal integrity (SI) becomes an increasing challenge. Today, SI is typically addressed late in the design process after the PCB layout has been completed by performing complex and time-consuming 3D extractions and simulations for high-speed lines.

But with little attention being paid to SI during the layout process, the simulation frequently identifies numerous SI problems. Multiple design and simulation iterations are often required to resolve these issues, in some cases causing delays in bringing the product to market and increasing nonrecurring expenses. An embedded SI checker helps by automatically checking for common mistakes that frequently cause SI problems such as missing shielding, return path discontinuities, ground or power loops, impedance mismatches, etc. Even with this approach, simulations are still required as a final check, but reducing the number of issues that must be addressed at this late stage helps bring the product to market faster and reduces engineering costs.

SI Design Challenges

Increasing data rates, higher IO counts and greater design complexity are leading to greater challenges in meeting SI and electromagnetic interference (EMI) requirements. For instance, 3DIC technology utilizes through-silicon vias (TSVs) to eliminate bond wires and further reduce interconnection distance in stacked chip configurations, providing higher speed performance and lower power consumption at the cost of creating many new opportunities for harmful radiation. Meanwhile, regulatory authorities are tightening electromagnetic compatibility (EMC) requirements by requiring compliance at higher and higher frequencies. The trend towards integrating multiple radios—each of which is an intentional radiator—into electronic products creates further challenges.

But the complexity of today's designs and the high levels of automation required to complete them in a reasonable time period usually prevent electrical designers from paying more than cursory attention to SI during the design process. Nearly all PCB design tools have built-in design rule checkers (DRCs) but they typically evaluate the design from a manufacturability perspective, rather than from an SI perspective. Simulation is normally performed after the design has been completed, when it becomes pos-

Meeting the demands of the latest LED lighting designs delivering an unprecedented level of thermal performance

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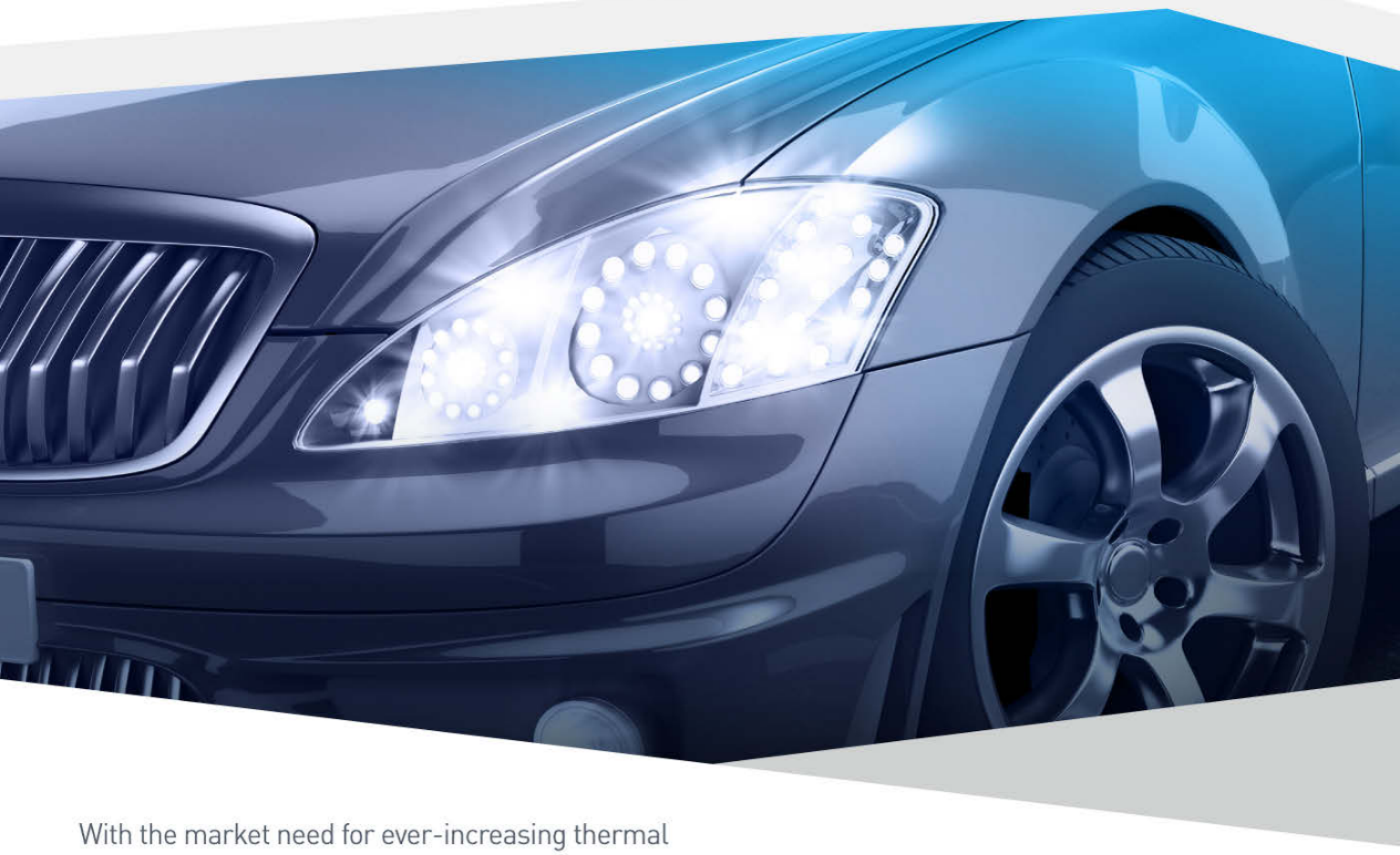

With the market need for ever-increasing thermal performance, the Ventec VT-4B family of thermally conductive IMS (Insulated Metal Substrates) deliver an unprecedented level of thermal performance through their established ceramic-filled halogen-free dielectric technology. Multilayered constructions are made possible through resin-coated foil and resin-coated film options.

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sible to model its performance by calculating a 3D solution of Maxwell's equations, which provides an elegant mathematical representation of electromagnetic interactions. The result, all too often, is that large numbers of SI problems are identified at a point relatively late in the design process when changes are very expensive to make. As a general rule, the cost of design changes generally increases by an order of magnitude or more as the design moves from conceptual to detailed to simulation.

SI Checkers use Configurable Rules

The latest generation of PCB design solutions, such as Zuken's CR-8000, incorporate features like an SI checker in the form of EMC advisor that evaluates the design during the layout process to predict, analyze and control issues that may cause SI or EMC problems. An embedded field solver calculates characteristic impedance, unit length delays and the mutual inductances and capacitances between lines. The SI checker runs as a menu item without requiring external net or components lists, exchange files or translators. Users can configure each rule by assigning specific parameters to nets. This is important because every board design has its own unique tradeoffs between performance, cost and schedule, not to mention corporate culture.

The ability to configure rules enables users to take control over the process and adopt the rules to the needs of the specific project. The user can weight rules so that some are considered more and others less important in the overall design rating. The user can also evaluate what-if scenarios by changing parameters globally and updating the rule checks. Files are provided to identify potential problems at the earliest stage possible in order to minimize the effects of design changes, reduce overall development cost, and speed up the design cycle.

Common Design Mistakes

Shielding: Sensitive circuits such as clock and high-speed signal wiring often require shielding to protect them from nearby radio frequency (RF) fields. As an example, CE testing, which is required to sell products in the European Union, for example, typically subjects electronic products to a radiated field of 1 V/m to 10 V/m magnitude over a 80 MHz to 6 GHz frequency range. Some industries such as automotive and aerospace are required to withstand even more difficult tests. This RF energy may couple to sensitive circuits such as clock and high-speed signal wiring and induce voltages and currents that can adversely affect its performance. The SI checker inspects shields near applicable signal vias. When the shielded level is below the parameter set by the user, the design feature is called out. The rule checker recommends an appropriate remedy for each fault such as applying an appropriate shielding to the object net patterns, placing appropriate

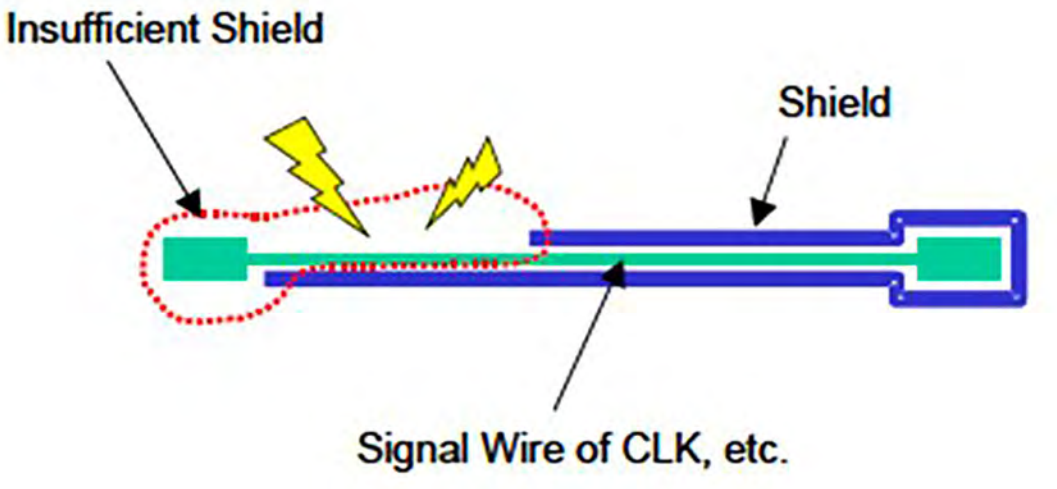

Figure 2: Trace shielding check.

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shield vias near the applicable net vias and connecting the shields to ground or power.

Return path discontinuity: Signal currents always take the path of lowest impedance, creating the potential for them to flow in unexpected directions, resulting in what is called return path discontinuity. When the return path forms a loop, the result may be increased delay in signal transmission or radiation that can interfere with other circuitry in the device or violate EMC regulations. The general rule of thumb is to minimize loop areas formed by return current for high-frequency signal, power and clock circuits. The SI checker identifies the target signal path, the wiring path connecting the target terminal pair, and the return path, the path closest to the target signal path between driver sound ground terminal and receiver side ground terminal. Next, the checker looks for an inappropriate return path, one that is not on the same layer or next layer as the return path or one that exceeds the permissible distance from the return path. The rule checker then calculates the severity of the loop based on the following formula: error rating = 1 – (error path length + return path length).

Impedance mismatch: Transmission lines become increasingly prone to noise as signal speed increases. In particular, mismatches between the trace's characteristic impedance and the driver's output or load's input impedance create signal reflections. These reflections in turn generate negative effects including radiation noise. Wiring width change is one of the factors that cause impedance mismatches. The SI checker calculates the characteristic impedance by finding the closest reference planes above and below the circuit. Wirings in the same layer are divided into sections and calculated separately when they have different reference planes.

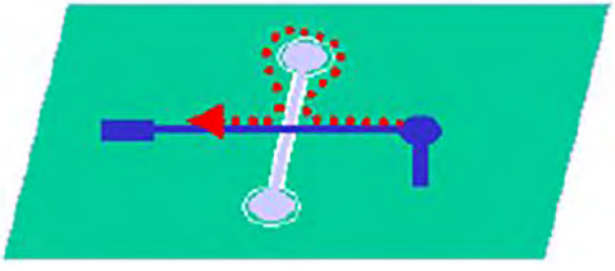


Figure 3: Return path discontinuity check.

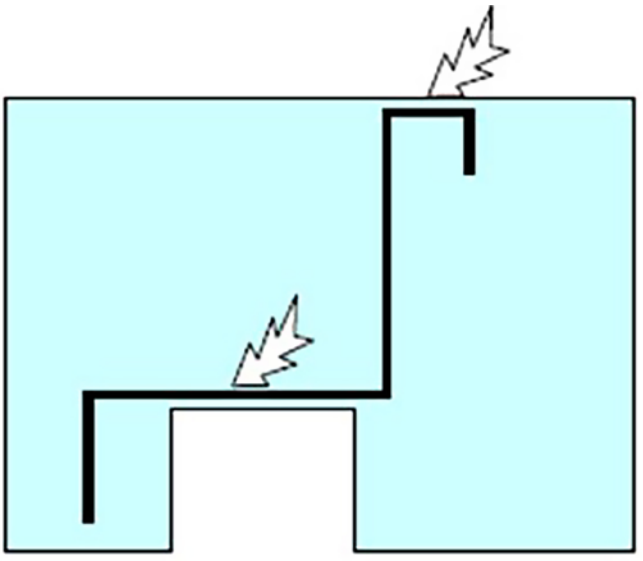


Figure 4: Trace near the plane edge.

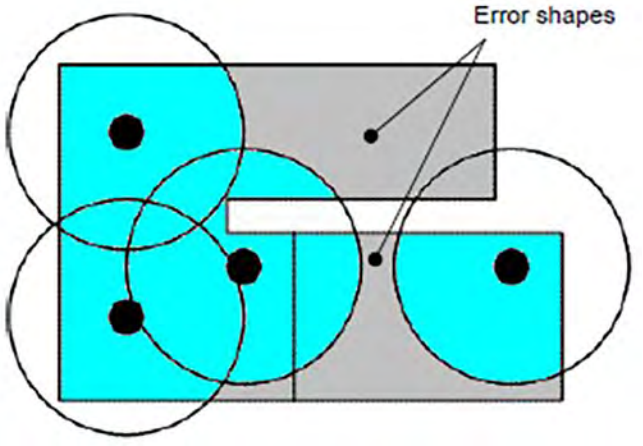


Figure 5: Plane via distribution.

High-speed signal wiring too close to the edge of a reference plane can also generate noise. The EMC advisor identifies wiring with frequency, rise time and voltage amplitude values that exceed user-specified parameters. Thus, the SI checker identifies potential risks for high-speed signals that may be prone to increased radiation noise.

Via density: If there are not enough vias distributed with sufficient density within any given area of a power or ground plane, the po-

tential exists for this area to function like an antenna and generate unwanted radiation. In addition, lack of reference path vias may cause longer return loops and also contribute to increased simultaneous switching noise. The rule checker checks to see whether or not padstacks are distributed in the plane with sufficient density. It operates by marking off sections within a user-defined radius of the center of each via. The sections that have not been marked off are considered to be problematic and when the ratio of problematic to good sections reaches a specific level in an area, then that area is called out by the rule checker.

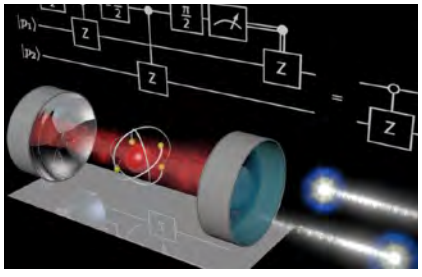
The SI checker also identifies many other mistakes that might be made in the design layout such as track resonance, EMC incompatible layer stack, isolated copper areas, overlapping power planes, high power plan impedance, etc. After running the selected rules, results are presented to the user in a graphical histogram. This also shows the results as a percentage performance rating and uses a custom color code to reflect the seriousness of the problem. Once the rules have been run, the issues that have been detected can be highlighted in the PCB design. Complete control of the highlighting is available for any combination of rules and design items within the rules.

Conclusion

The benefit of performing layout-level SI checks is that the need to iterate through time-consuming model extraction and simulation is reduced, as the simulation will identify far fewer SI issues or perhaps none at all. By identifying SI issues early in the design process when they can be corrected in much less time and at a much lower cost than after the design has been completed, upfront SI checking can reduce time to market and engineering costs. **PCBDESIGN**

Narayanan TV is a solutions architect at Zuken USA where he helps define chip/package/board co-design solutions with a focus on signal and power integrity.

Quantum Processor for Single Photons



"Nothing is impossible!" In line with this motto, physicists from the Quantum Dynamics Division of Professor Gerhard Rempe, director at the Max Planck Institute of Quantum Optics, managed to realise a quantum logic gate in which two light quanta are the main actors.

To realise a universal quantum computer, it is necessary that every input quantum bit can cause a maximal change of the other quantum bits. The practical difficulty lies in the special nature of quantum information: in contrast to classical bits, it cannot be copied. The realisation of a deterministic photon-photon gate has been a long-standing goal. One of several possibilities to encode photonic quantum bits is the use of polarisation states of single photons. Two independently polarised photons impinge, in quick succession, onto a resonator which is made of two high-reflectivity mirrors. The resonator amplifies the light field of the impinging photon at the position of the atom enabling a direct atom-photon interaction. As a result, the atomic state gets manipulated by the photon just as it is being reflected from the mirror. This change is sensed by the second photon when it arrives at the mirror shortly thereafter.

After their reflection, both photons are stored in a 1.2-kilometre-long optical fibre for some microseconds. Meanwhile, the atomic state is measured.

The case when the input polarisation of the two photons is chosen such that they influence each other is of particular interest: Here the two outgoing photons form an entangled pair. The scientists envision that the new photon-photon gate could pave the way towards all-optical quantum information processing.

Having Fun With Impedance

by Abby Monaco
INTERCEPT TECHNOLOGY

About a year ago, I was assigned a new project: become an expert in impedance, more or less. I had no idea how much this research would bring out the nerd in me. I'm still not an impedance guru, but I've learned a lot about how impedance requirements affect PCBs.

Even if you don't typically design controlled-impedance circuit boards, you probably will eventually. Fortunately, designers have access to impedance software that takes care of the heavy lifting.

Let's start at the beginning. According to Wikipedia, "Electrical impedance is the measure of the opposition that a circuit presents to a current when a voltage is applied." Makes perfect sense, doesn't it?

Obviously, the definition of impedance doesn't really tell us what it means to designers and engineers. As high-speed designs continue to push into ever faster envelopes, the tools used to analyze electromagnetic interference (EMI), signal integrity (SI), and impedance are becoming more and more crucial to executing a successful, sustainable design.

As an electrical engineer co-worker said, "It's not whether the design works. It's whether it can work better." A great example of this is how the airlines are now starting to allow cell phone usage in the sky. With aeronautical equipment and mobile devices becoming more streamlined, with far less noise emitted in either direction, there are fewer chances that the frequency of a cell phone will collide with the frequency of the airplane's instruments. Providing this convenience to passengers is a milestone not only for the airlines, but also for all of the software programs that support the careful, iterative improvements made upon older design concepts. (Just don't talk non-stop on your cell phone if you're sitting next to me.)

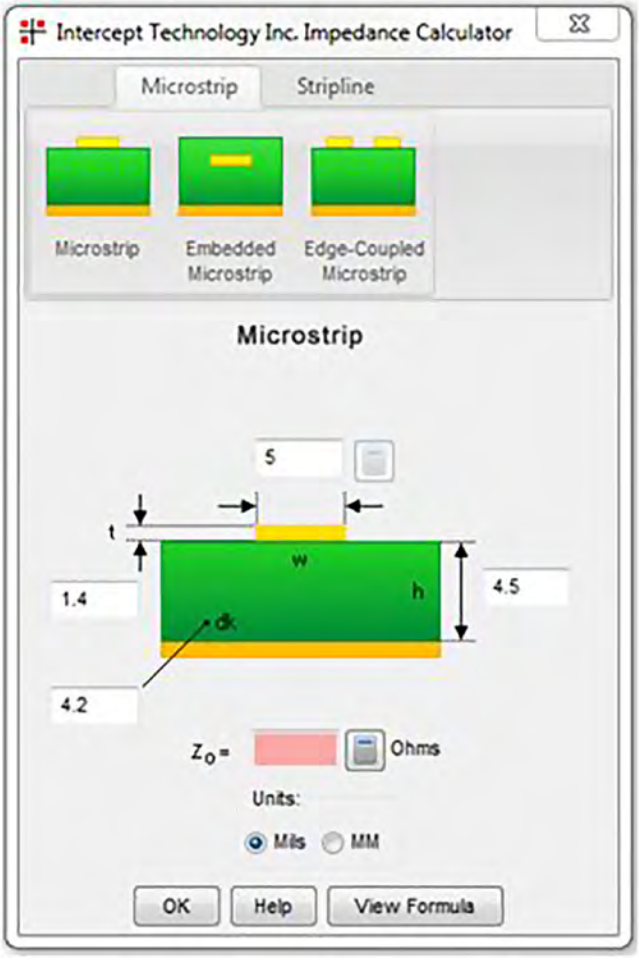
So, you've put the finishing touches on some of your beautiful hand routes, only to have the engineer come ask you to switch out your resistors for a different value, and space out your wires by .005" instead of .004". Don't take it personally; your engineer is just trying to preclude any impedance issues.

In my journey to learn everything I could about impedance, I had the joyful experience of working with some of the best and brightest software engineers around. In the process, we've come up with the coolest impedance calculator I've found yet, available as an app for the Droid and the iPhone. Yes, you can download this fabulous gem and impress all your industry colleagues with your knowledge of microstrip and stripline impedance calculations.

Some of you already have a solid understanding of impedance calculators. But even if you're far from an expert in this arena, an impedance calculator can help you take this:

$$Z_o = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98H}{0.8W + T}\right) \text{ ohms}$$

And turn it into this:



Just look at it. Don't you want to use it right now? Our impedance calculator allows you to determine your wire widths based on your dielectric heights, or the other way around. Building the stack-up and the design rules have suddenly become fun. I am as much in love with my TI calculator as the next electronics geek, but having an app that can calculate both backward and forward gives you the ability to really focus on the end-goal instead of checking and rechecking your work. It's a fantastic productivity booster.

But what I became acutely aware of during this project, first and foremost, is that designers must always exhibit great patience. The process of beginning a brand new circuit design never has a defined point A and point B, and no real start and finish. It is just as circuitous as the finished design displays; while one engineer is off calculating impedances, another one may be calculating signal integrity or EMI. The board designer may or may not be aware of what these engineers are doing, all the while being right in the middle of placement and routing processes.

This is often the source of that familiar frustration with the "us" and "them." So when you're putting the finishing touches on your beautiful hand routes and the engineer comes back and asks you to switch out the resistors for a different value, and space out your wires by .005" instead of .004", take a deep breath and try to recognize why!

These design changes can be caused by numerous drivers, such as heat dissipation, electrical interference, or too much "noise." These issues can be controlled in a variety of ways, such as using different valued resistors to dampen the speed of the signal, shielding areas of circuitry from the rest of the design, or carefully distributing properly sized heat sinks throughout the design. Sometimes the solution to the problem feels like an artistic swipe of a brush in a very square and confined space, in a perfect marriage of the logical and the creative.

While patience is an important value for us as designers, I must also highlight that humility is key. Just when you believe you have become the expert on a topic, you will come to find that there is so much more to learn. Five years from now, we'll still be learning new methods for de-

signing for signal integrity, and our EDA tools' algorithms will be honed and improved even more. Five years from now, I bet we'll be turning our noses up at the Intercept Impedance Calculator app of today, in favor of something entirely more sophisticated.

If you have any comments on how to better use controlled impedance to reduce noise, hot spots, or any other design flaws, let me know. I'd love to hear from you! **PCBDESIGN**

To download the Google version of the Intercept Impedance Calculator, click here. The iOS version is available by clicking here.

Abby Monaco, CID, is with Intercept Technology Inc. and has 15 years of experience in EDA

Automotive LED Market Has a Bright Future With the Rise of Replacement Products

The value of the global LED market has been growing at a crawling pace as demand for backlight LEDs contracts. Automotive LEDs, however, are one of the few sizable application markets that are developing rapidly. The latest analysis by LEDinside, a division of TrendForce, finds the replacement of traditional light bulbs with LED light sources continues steadily in the automotive lighting market despite the slowing growth in the regional automobile markets worldwide during the second quarter. LEDinside projects that the value of the exterior automotive LED market will reach US$1.57 billion this year and will grow at a CAGR of 6% in the 2016~2020 period.

In the case of China's automotive lighting market, Duff Lu, research manager for LEDinside, said the use of LEDs is still mainly influenced by cost considerations. Hence, the penetration rates of LEDs in China's interior automotive lighting and rear position lamp segments are now over 70%, respectively. Chinese automotive lighting manufacturers have also made rapid progress in the technological development of daylight running lights (DRLs) in recent years and some have begun to use standard LEDs for their DRL products. LEDinside projects that the penetration rate in China's DRL segment will reach 47% in 2016. As for high-power LED packages used for high and low beams, Chinese manufacturers still rely on imports because most domestic suppliers are not mature enough technologically to produce these components. Hence, LED penetration rate China's high/low beam market is currently less than 3%.

Lu pointed out replacing traditional light bulbs in an automotive luminaire can only be done by opening up the luminaire's back cover and pull the light bulbs out from their sockets. However, LED products tend to be integrated or systematic in design and most LED automotive lighting products in the OEM market come as an entire luminaire assembly. They thus are not suited for the conventional replacement method. To expand the adoption of LEDs, LED module suppliers are developing replacement or plug-in light bulb products that can substitute traditional light bulbs in an automotive luminaire.

PCB007 Highlights

Weiner's World

Gen Consulting Company (GCC) has issued the Radiant Insights report "Global HDI Printed Circuit Board Market Forecast and Analysis 2016–2021." The report provides a detailed analysis of worldwide markets for HDI printed circuit boards from 2011–2016, and provides market forecasts for 2016–2021 by region/country and subsectors.

EIPC Summer Conference 2016, Day 2: Strategies to Maintain Profitability in the European PCB Industry

Delegates awoke to a gloomy Scottish morning on the second day of the EIPC Summer Conference 2016. One or two who maybe overindulged in the whisky on the previous evening had some difficulty in finding time for breakfast before the conference proceedings, but the atmosphere in the meeting room was brighter than the weather outside, as Professor Martin Goosey introduced the day's programme.

Graphic PLC…Are the Rumors True?

During a visit to Europe recently, I-Connect007's Barry Matties met with Rex Rozario to get to the bottom of the rumors and speculation regarding the sale of his company, Graphic PLC.

Happy's Essential Skills: Learning Theory/ Learning Curves

Learning is not instantaneous. Nor is progress made in a steady manner, but at a rate that is typified by one of two basic patterns. In some cases, plateaus will be seen in learning curves. These are caused by factors such as fatigue, poor motivation, loss of interest, or needing time to absorb all the material before progressing to new.

EIPC Summer Conference 2016, Day 1: Strategies to Maintain Profitability in the European PCB Industry

Resplendent in the kilt, EIPC chairman Alun Morgan welcomed a large and enthusiastic gathering of printed circuit professionals from all over Europe and as far afield as the USA, Canada and Russia, to the EIPC Summer Conference 2016 in Edinburgh, Scotland's cosmopolitan capital city.

Institute of Circuit Technology Annual Symposium

On June 1, Technical Director Bill Wilkie introduced the 42nd Annual Symposium of the Institute of Circuit Technology, at the Motorcycle Museum in Birmingham, UK, commenting upon the success of the recent Foundation Course and acknowledging the sterling efforts of his course tutors, although recognising that some of his longest-standing experts were now retiring.

It's Only Common Sense: Elevate the Conversation to get Closer to your Customers

So we all think we are doing a pretty good job getting to know our customers, right? We think because we know what market they are in and what they build, and have some sort of idea of what they need we are in pretty good shape, right?

All About Flex: Flexible Circuit Fabrication and Cleanroom Manufacturing

Facility cleanliness is a vital part of process control for flexible circuit fabricators. As higher density requirements continue a relentless drive toward finer traces and spaces, particles and foreign material can cause problems in a number of operations.

Standard of Excellence: LED and Metal-Backed Technology—Today and in the Future

Probably one of the hottest, or should I say coolest, technologies today is LED. I would also venture to say it is one of the fastest growing as well. All you have to do is look around you can see evidence of this everywhere from holiday lights in your home and Jumbotrons at sports arenas, to highway and business signage. The lighting industry is now dominated by LED technology.

Flexible Electronics Market to Reach $87.2 Billion by 2024

The global flexible electronics market was $20.85 billion in 2015, which is estimated to reach $87.2 billion by 2024, according to a new report by Grand View Research, Inc.

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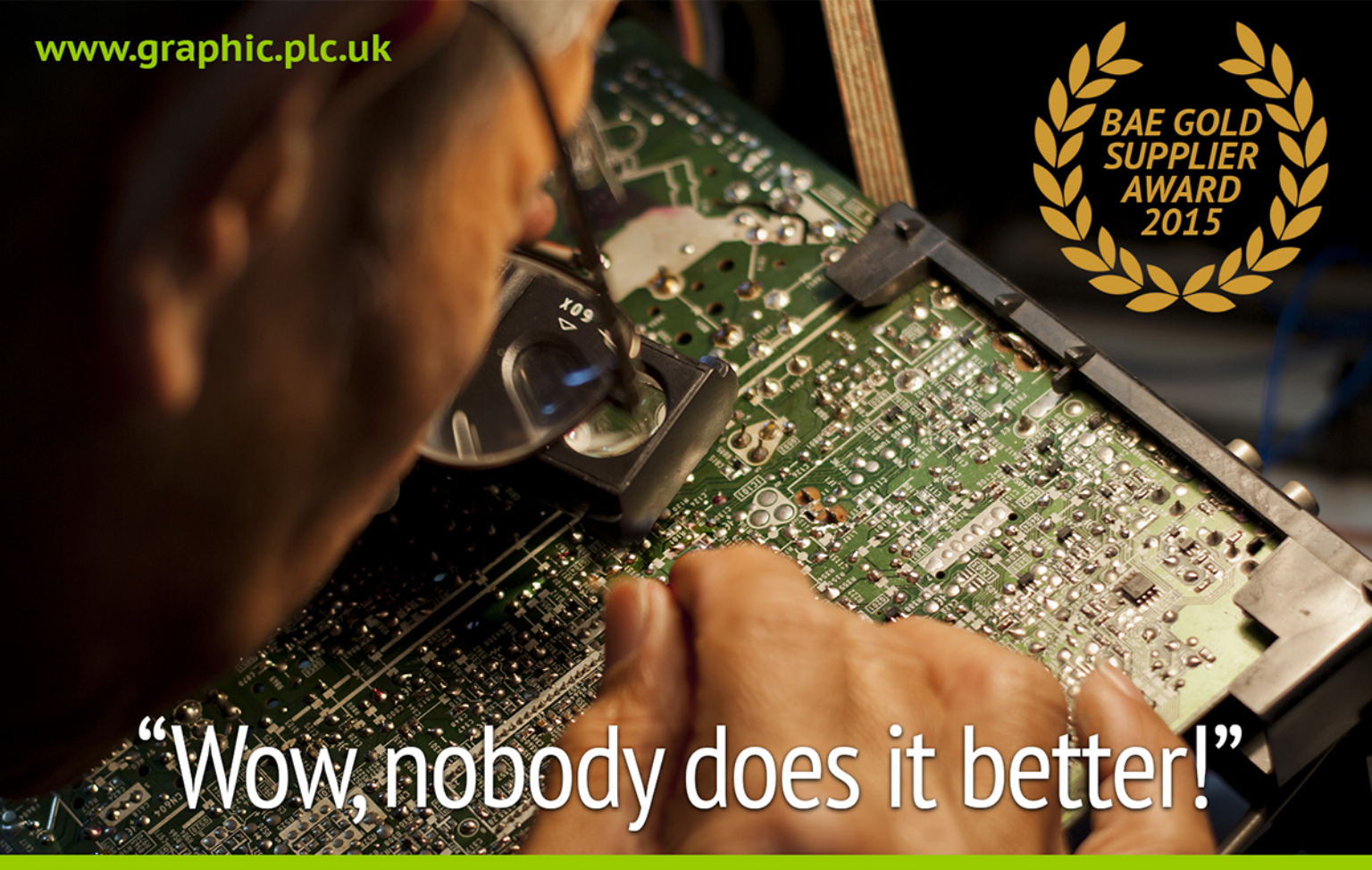

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The Rise of the Independent Engineer

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

With the changing demographics, the old-timers in our industry—the master PCB designers—are about to retire and hand over the exacting job of PCB design to the Gen-X and Ys. These generations, shaped by technology, will tackle the most demanding designs without possessing the experience that we veterans benefit from.

And to top it off, these up-and-coming designers will be degreed engineers who have to cope with both design and layout tasks as the specialized PCB designer's positions are phased out. Apart from a demanding regime of training, what can these guys do to become successful independent engineers?

The majority of veteran PCB designers began their careers on a drafting table. In the late 1970s, basic PCB design software began to emerge in the mainstream market. The computer skills of the PCB designer grew and before you knew it, we were all proficient with the latest EDA software tools. Some argue that since the emergence of EDA, the line between layout and engineering has become blurred. Engineers who are proficient with EDA software can produce a complex PCB, eliminating the need for a PCB designer. Similarly, a PCB designer can perform engineering design with the use of sophisticated analysis software. In theory, this is a good concept but from the engineer's perspective, it runs into practical problems:

1. Engineers must undergo significant training in order to use the software. In many cases, this is simply not feasible and the lost opportunity costs are prohibitive.
2. In order to remain proficient, the engineer must regularly use the software. This is a problem for busy engineers who have a variety of responsibilities and only work on one or two projects per annum.
3. The engineer must have a thorough understanding of the specific requirements of the

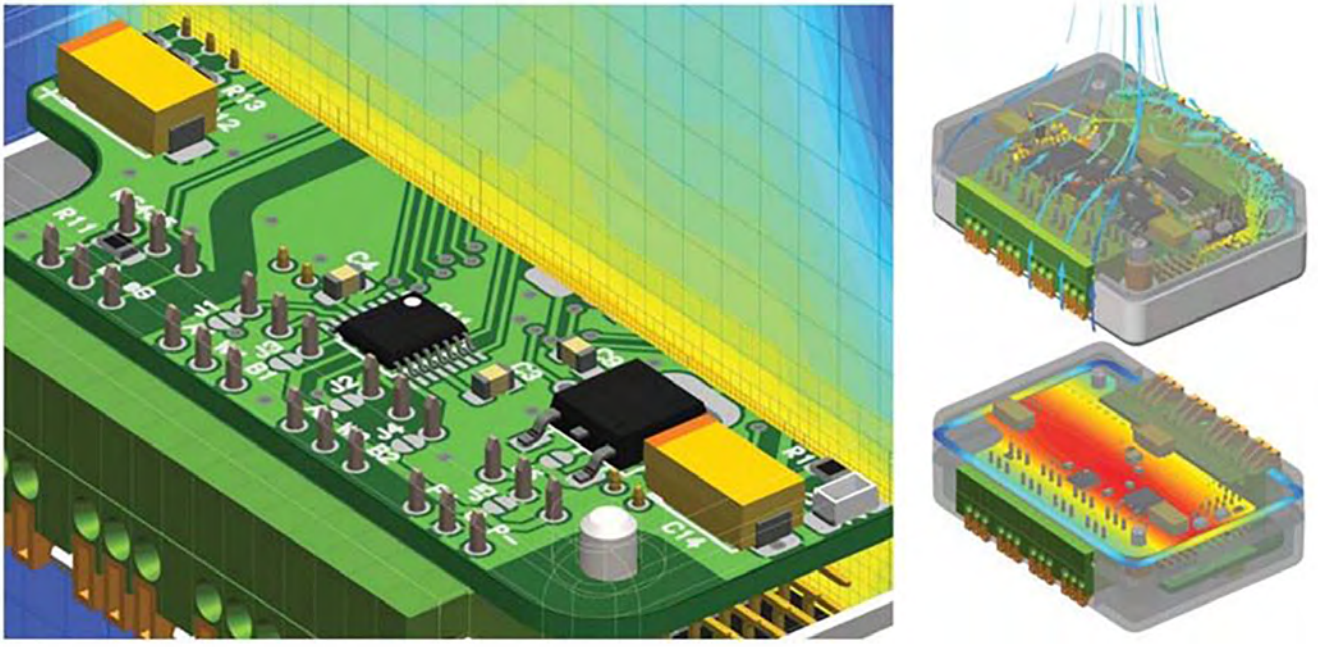

Figure 1: Thermal analysis of the PCB and assemblies. (All images courtesy of Mentor Graphics)

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The standard for the Internet of Manufacturing (IoM) has arrived!

The Open Manufacturing Language (OML) is a real-time communication standard for PCBA manufacturing that defines the interconnectivity of assembly production processes and enterprise IT systems.

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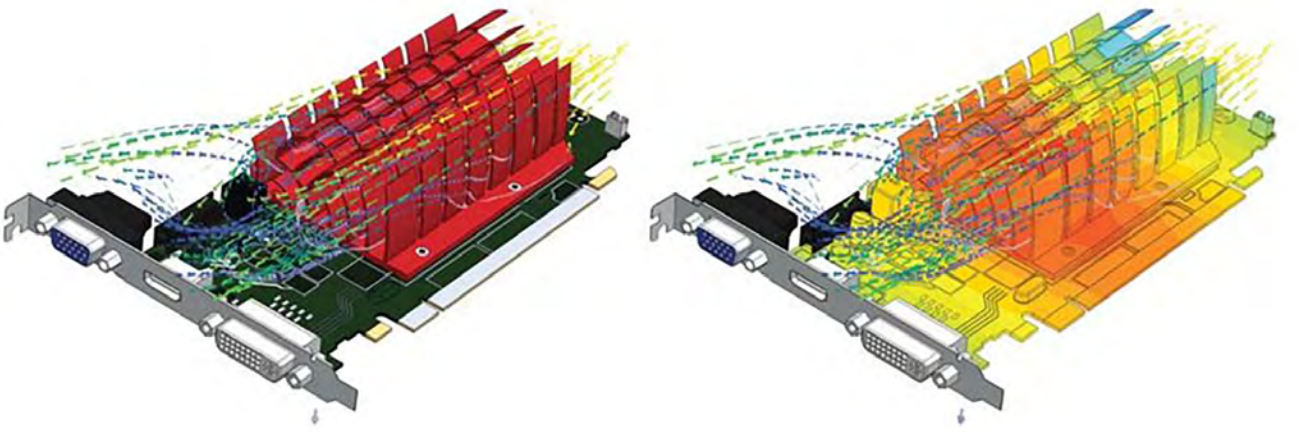

Figure 2: 3D flow field using particle post-processing.

design rules encompassing PCB fabrication and assembly in order to produce a reliable, manufacturable product.

The net result is that the engineer typically does not use the software but rather relies on the PCB designer's application and manufacturing knowledge to guide him through the process. Also, in most cases, the PCB designer struggles to use the analysis software and requires extensive and ongoing training. So, the next innovation in EDA tools must not only be fast to adopt and easy-to-use, but still be packed with all the features today's designers need for the most complex boards.

In the past, engineers were alienated from the layout tools. Many stood over the shoulder of the PCB designer, providing input during the design phase. This methodology is inefficient. It limits the engineer's ability to try alternate scenarios. However, the next generation will take control of the mouse which will enable them to make better design decisions. This may well be a positive aspect, as design complexity, with fast rise-time signals, reaches the point where high-speed digital circuits exhibit RF behavior. Engineers, unlike traditional PCB designers, are more aware of the transmission line issues including signal and power integrity requirements and can investigate the options that are available to them, on the fly, saving valuable development time.

Today, the PCB design process entails much more than just schematic capture and PCB layout. With increasing complexity in electronics systems, engineers need to develop with the whole product in mind. Having access to a design tool that encompasses PCB design, coupled with comprehensive simulation and analysis, really gives design engineers the confidence that their products will be delivered on schedule and at the highest performance and reliability.

To create a stable, reliable product, one must satisfy all the high-speed and manufacturing constraints. As electronic products become smaller, faster and more densely packed, engineers are compelled to consider thermal aspects (Figure 2) and utilize virtual prototyping to meet stringent schedules. Enter the product creation platform. Developed for individuals and small teams, designing electronic products, new tools such as the new Mentor Graphics PADS PCB product creation platform encompasses a variety of productivity enhancements.

The issues that previously impeded the independent engineer have been addressed by providing:

1. Professional layout tools that combine ease-of-use with highly automated functionality to give engineers exceptional control over the creation of the most complex designs. The familiar GUI enables the occasional user to pick it up and become productive quickly.

2. A powerful and easy-to-use constraint management system that provides a common, integrated constraint definition environment for the creation, review, and verification of PCB design rules. The system supports definition

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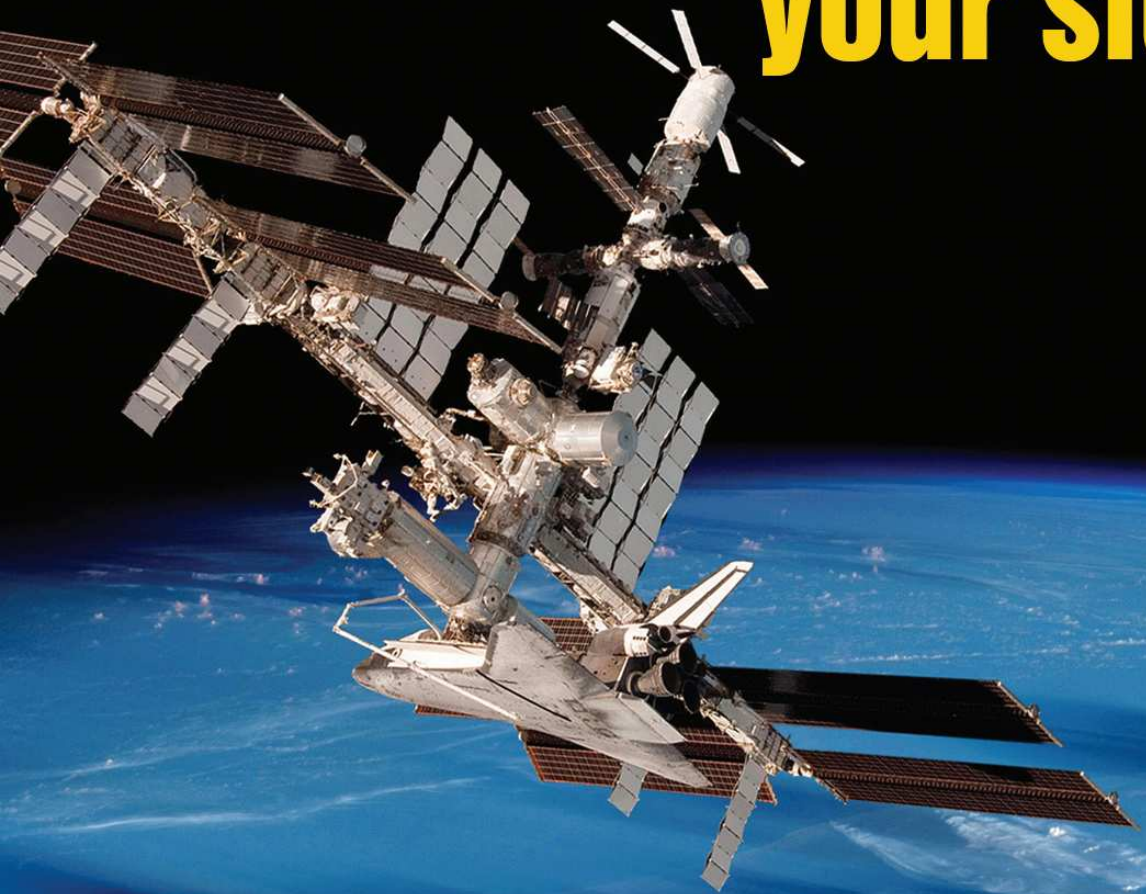

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and verification of electrical and physical constraints within one environment, eliminating the need for separate databases, and simplifying a complex constraint entry process while improving design accuracy.

3. Apart from ECAD-MCAD collaboration and EMC verification tools, tight integration with Valor NPI for concurrent DFM validation and optimized hand-off to manufacturing. This ensures that all manufacturing data is included and synchronized, and that the engineer's design intent is maintained. Additional, Valor NPI provides concurrent DfM analysis during the design process, applying almost 700 manufacturing rules, to the design, ensuring compliance and minimum revision spins in manufacturing.

With the release of the product creation platform, PADS has included the FloTHERM XT option that utilizes a powerful solver and mesher for fast and effective electronics cooling simulations, working with both MCAD and PADS design flows. Full geometric and non-geometric SmartParts and library capabilities provide access to a full set of the most popular components for fast and accurate model creation. You can easily define, solve, and analyze results using parametric variations of geometry, attributes (e.g., material, thermal), and solution parameters to significantly enhance the design optimization process.

The tight integration with PCB layout reduces time consuming data translation and prevents costly errors. Board or component layout can be easily modified for position, size, orientation, shape, and modeling level prior to import into FloTHERM.

Insufficient cooling can result in poor reliability, schedule delays, and increased production costs. This is especially relevant in today's high-performance devices where components are densely packed into ever-smaller enclosures. Proper thermal management, of the entire de-

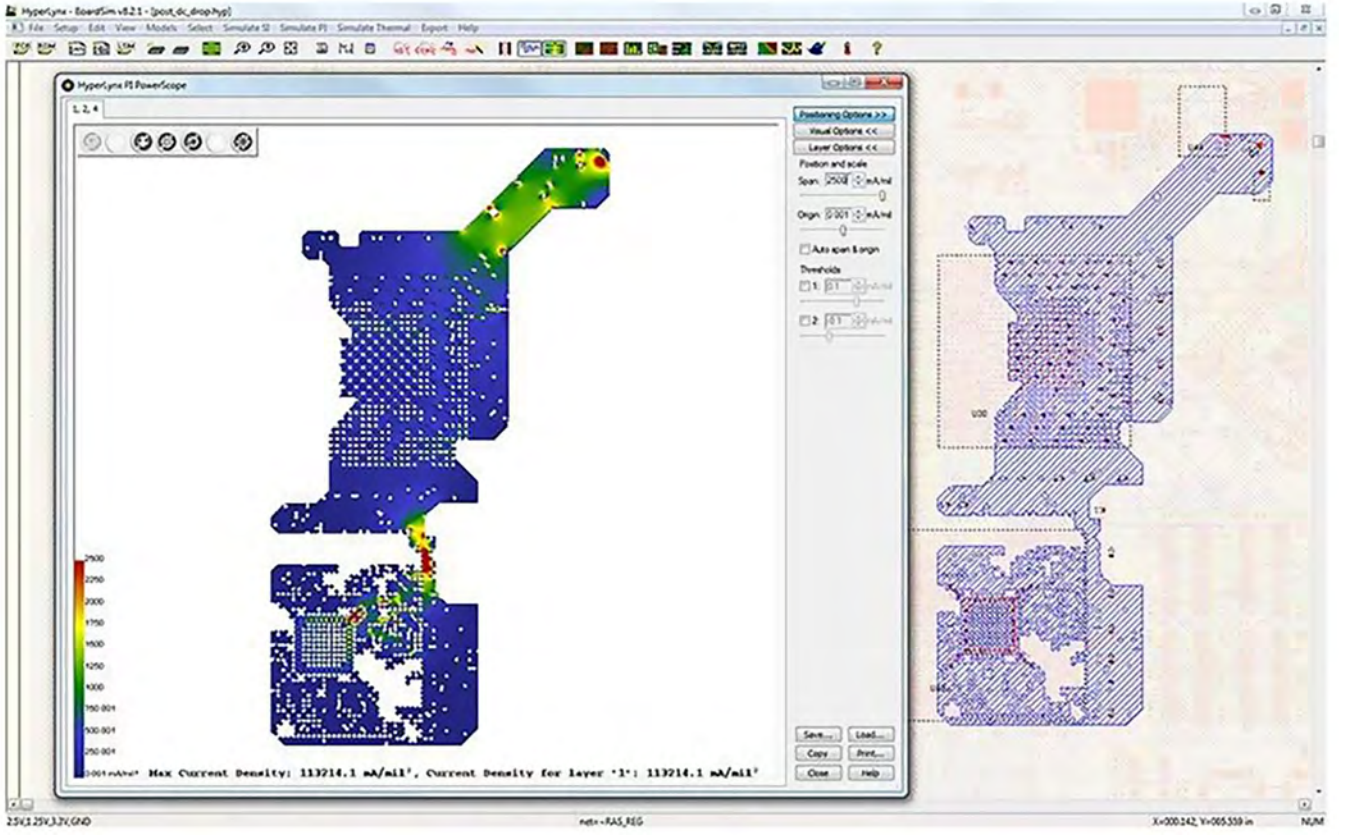

Figure 3: IR drop analysis identifies excessive current density.

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sign space, is essential to delivering on-time, on-budget, reliable electronic products.

Also, power delivery and reliability are critical for product creation with today's modern, high-performance digital circuits. Unpredictable, intermittent circuit behavior can be avoided by identifying power delivery issues early in the product creation process. The HyperLynx DC Drop power integrity analysis environment is easy to set up and use, giving simulation results without requiring weeks of software training. Power distribution problems can be identified early in the design, even prior to layout. IR drop issues (Figure 3) can be identified that would otherwise be difficult to spot in the lab, and solutions can be investigated in an easy-to-use "what-if" environment. Once the layout is complete, the results can be validated to ensure that the appropriate guidelines were followed. This will ultimately reduce prototype spins and deliver the product to market faster, while creating more reliable products.

One huge advantage the next generation has in their favor is the availability of information. I recall back in my day, we had to actually buy books and magazines to get technical information. But now, it is just a matter of uttering "OK Google" and a wealth of information is available at our finger tips. Imagine how much we old guys would know now if we had had access to such powerful search engines during our academic years? The even younger Gen Z is the first generation that never experienced the pre-Internet world. To them, a magazine is just an iPad that doesn't work.

Raised on high-technology, the next generation of PCB designer—the independent engineer—is very computer savvy and more adapt to manipulating the application software to achieve the outcomes they need. Given the ever decreasing time-to-market constraints imposed today, these guys are well equipped to tackle a multi-disciplined environment that increases design process efficiency. The younger generation has a lot to offer with new ideas and more efficient processes. Success is built on experience, but with the latest EDA tools that can provide automated features that cover the lapse in experience, the independent engineer will be empowered to push the envelope of design integration and complexity to the next level. **PCBDESIGN**

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1. Softree: Empowering Engineers with Easy-to-Use Civil Design Software
2. Mentor Graphics PADS documentation
3. PADS software information: www.pads.com

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD) Australia. The company is a PCB design service bureau that specializes in board-level simulation. ICD has developed the ICD Stackup Planner and ICD PDN Planner software, which is available here.

Rechargeable Batteries That Last Longer and Re-charge More Rapidly

Materials researchers at the Swiss Paul Scherrer Institute PSI in Villigen and the ETH Zurich have developed a very simple and cost-effective procedure for significantly enhancing the performance of conventional Li-ion rechargeable batteries.

When the battery is in use and thus discharging, the lithium ions pass back to the cathode but are forced to take many detours through the densely packed mass of graphite flakes, compromising battery performance.

These detours are largely avoidable if the flakes are arranged vertically during the anode production process so that they are massed parallel to one another, pointing from the electrode plane in the direction of the cathode. Adapting a method already used in the production of synthetic composite materials, this alignment was achieved by André Studart and a team of research experts in the field of material nanostructuration at the ETH Zurich. The method involves coating the graphite flakes with nanoparticles of iron oxide sensitive to a magnetic field and suspending them in ethanol. The suspended and already magnetized flakes are subsequently subjected to a magnetic field of 100 millitesla, about the strength of a fridge magnet.

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When Coatings Go Wrong

by Phil Kinner
ELECTROLUBE CONFORMAL COATINGS DIVISION

This month, I consider some of the more common, and often very frustrating, problems that may be encountered when coating electronic circuit boards and components. I also discuss some practical solutions.

As we all know, nothing in life is straightforward. In any engineering discipline, if there is the slightest chance that something might go wrong, you can bet your bottom dollar that it will. The secret is to be prepared for it. For the purposes of this column, I'm going to concentrate on the use of conformal coatings for the protection of electronic assemblies, highlighting some of the potential pitfalls associated with the choice of coating and the method of application. In each case, I will suggest an approach that should mitigate the majority of problems you are likely to encounter.

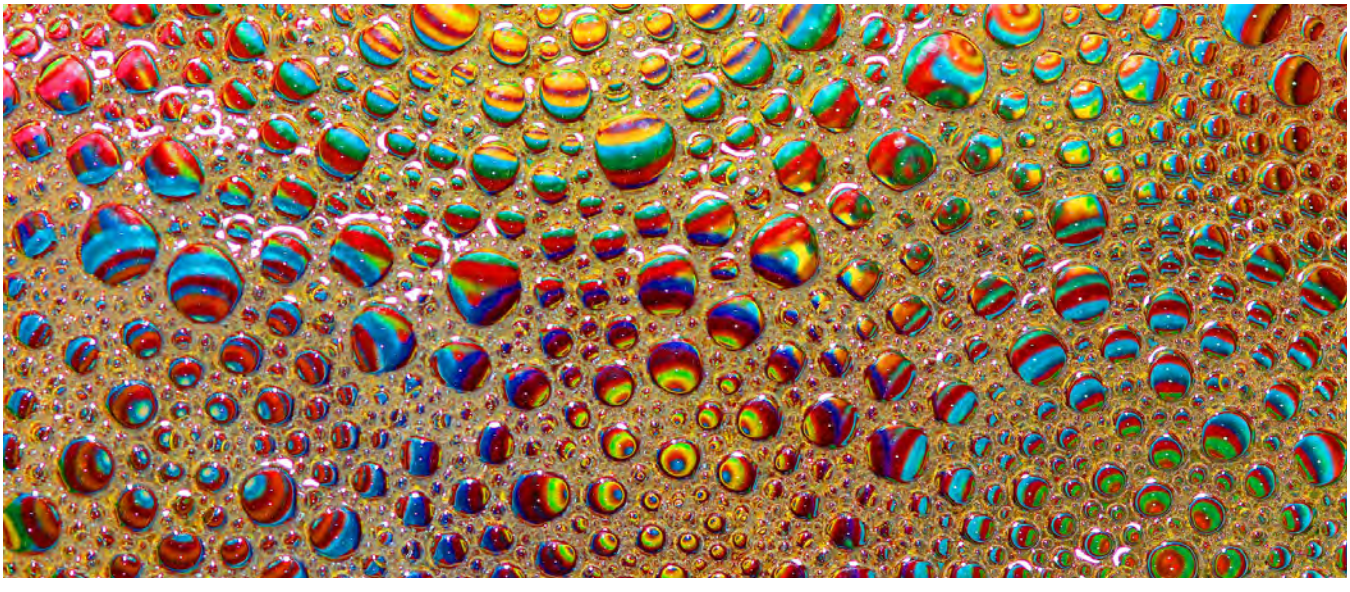
Problem: The quality and performance of a conformal coating material could be compromised according to the method of application.

This issue is commonly encountered when a product is transferred from one circuit manufacturer to another; for example, a product may be dip-coated in one country but selectively coated in another, with the specification requiring that the same material be used at both sites. The problem that arises here, however, is that using a material formulated for dip-coating in selective coating equipment can result in poor yield due to excessively fast drying and bubble entrapment.

One of my customers spent six months trying to solve a bubble issue internally, without realising that the root cause of this problem lay in the material formulation. After working with the customer, we found that by changing the solvent blend, the bubble entrapment issue could easily be resolved. Moreover, this solution simplified the process and reduced the cycle time. And since the non-volatile formulation remained the same, there was no need to re-qualify.

Problem: Achieving incorrect coating thickness, especially with acrylics.

The IPC specification allows a dry film thickness of between 30 and 130 microns, with the greater thickness being achieved by the application of multiple coating layers. Trying to achieve a 130-micron dry film thickness from a



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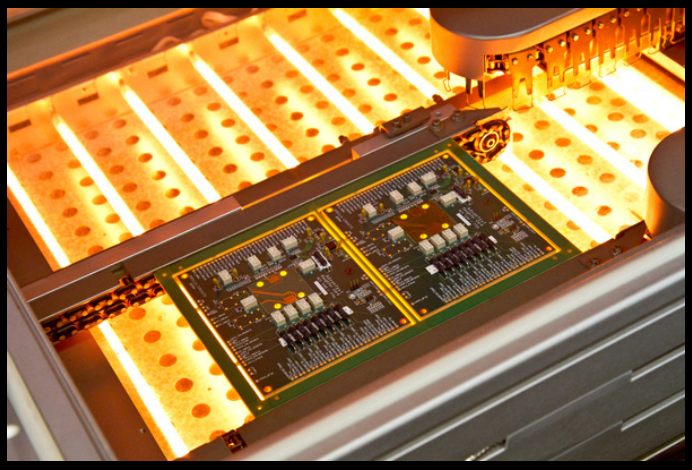

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single selective-coating process with a solvent-based acrylic material is a recipe for a disaster, likely to result in excessive bubble formation, film shrinkage, coating delamination and additional stress on components. The result is poorer protection, rather than an improved overall level of circuit protection. Aiming for a uniform 30-50 microns and focusing on achieving perfect coverage at each application is a much better approach to improving the protection of electronic circuits.

Achieving the correct coating thickness is important; bear in mind that if the coating is too thick it can lead to entrapment of solvents in areas where the coating does not fully cure. Similarly, it can cause the coating to crack as it cures or as the result of changes in temperature, or due to mechanical shock and vibration.

Problem: Liquid conformal coatings are subject to strong capillary forces from low standoff components such as passives, as well as BGA, QFP and QFN style packages.

If a conformal coating is applied too thickly or at too low a viscosity, the material can be sucked underneath components, leading to a non-uniform fluorescence (some coatings contain a fluorescent dye that allows blacklight inspection of the PCB after coating to ensure complete and uniform coverage), as well as potential issues with package reliability. If the material takes too long to dry, the same phenomena can be seen.

Some solvent-based conformal coatings can be difficult to inspect by fluorescence when the coating thickness is 20 microns or less. The temptation is to apply more material, which can exacerbate the component reliability issue due to coefficient of thermal expansion (CTE) mismatches in the Z direction. Increasing the viscosity and the rate at which the material builds viscosity can help to improve uniformity.

While it may involve some double handling or the inclusion of an additional process, an alternative approach is to apply a thin "primer" coat layer. This will improve the ability of the coating to cover sharp, vertical edges of components and reduce the likelihood of bubble entrapment and capillary force effects during the main coating layer application.

Problem: Ambient temperature and its effect on the viscosity of liquid conformal coatings.

Some factories can have a 10-15°C temperature differential between mid-summer and mid-winter. Flow-cups are often used to control the dilution of material prior to use. Material blends with the same flow time in winter may be very different in their make-up to the summer blend, leading to a different set of process parameters, thickness, coverage, degree of uniformity achieved and so on. The best way to overcome this problem is to ensure that temperature measurement is included along with flow-time in the viscosity monitoring process.

Problem: Using "off-spec" thinners can lead to incompatibility issues with conformal coatings.

A recent customer experienced a problem with his conformal coating material appearance changing from clear/transparent to yellow hazy/cloudy, with a wrinkly and "de-wetted" finish when dried. Upon investigation it transpired that, in wishing to reduce his overall process costs, the customer had resorted to the use of paint thinner purchased from a local hardware store. The paint thinner was not compatible with the conformal coating formulation, a fact that came to light initially with the formation of a cloudy solution, and which was further suggested by the appearance of pin holes, confirmed by the wrinkled finish. Indeed, within 30 minutes of mixing the solution, it formed two layers!

In summary, while it might be tempting to use shortcuts either to reduce costs or to speed production, there will inevitably be a higher price to pay. Know the limitations and/or special properties of the materials you use to coat electronic assemblies and abide by the correct procedures. **PCBDESIGN**

Phil Kinner is technical director for Electrolube's Conformal Coatings Division.

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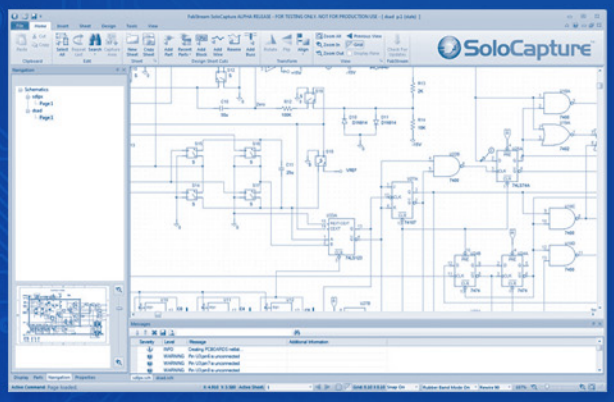

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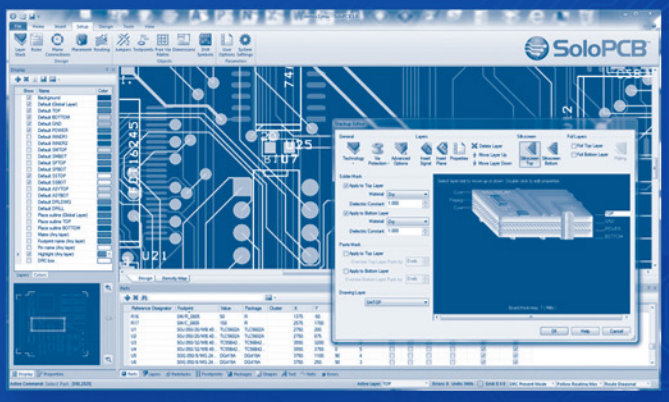

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MilAero007 Highlights

Global Technology Development: HDP User Group European Meeting 2016

Delighted and honoured to be invited again to attend the open session of the High Density Packaging User Group (HDPUG) European Meeting, I made my way to the picturesque Grand Duchy of Luxembourg, a tiny principality bordered by Belgium, France and Germany, and ranked among the world's top-three nations in both wealth and wine consumption.

What You Probably Don't Know about NASA

While at Maker Faire 2016 in San Mateo recently, I met with George Gorospe of NASA's Ames Research Center to discuss his group's recent findings and projects, NASA's CubeSats and microsatellites, and what the commercialization of space travel means for the near future.

IPC Standards Committee Reports, Part 2—Assembly and Joining, Component Traceability, Flexible Circuits, High Speed/High Frequency

These standards committee reports from IPC APEX EXPO 2016 have been compiled to help keep you up to date on IPC standards committee activities. This is the second in a series of reports.

Illinois Researcher Receives DARPA Contract to Design a Hybrid Robot

Illinois researcher Hae-Won Park has been awarded a Robotics Fast Track contract from the Defense Advanced Research Projects Agency (DARPA) to design a hybrid robot that can glide, land, and walk.

International Partners Provide Science Satellites for America's Space Launch SLS Maiden Flight

NASA's new Space Launch System (SLS) will launch America into a new era of exploration to destinations beyond Earth's orbit. On its first flight, NASA will demonstrate the rocket's heavy-lift capability and send an uncrewed Orion spacecraft into deep space.

Saab Receives Order within AEW&C Segment

Defence and security company Saab has landed an order within the Airborne Early Warning and Control (AEW&C) segment worth about SEK 1.1 billion.

American Standard Circuits Enhances Via Fill Capabilities with Double Systems

Anaya Vardya, CEO of American Standard Circuits, has announced that his company recently enhanced their via fill capabilities with the installation of a MASS VHF300 horizontal hole filling system with full chamber vacuum capability, accompanied by a MASS ES10 double-sided Scavenger unit.

Record-breaking $65B Global Defense Trade in 2015 Fueled by Middle East and Southeast Asia

"The global defense trade market has never seen an increase as large as the one we saw between 2014 and 2015," said Ben Moores, senior analyst at IHS. "2015 was a record-breaking year." Markets rose $6.6 billion, bringing the value of the global defense market in 2015 to $65 billion. IHS forecasts that the market will increase further to $69 billion in 2016.

BAE Systems Harnesses Pioneering Technology to Power Land Rover BAR's America's Cup Bid

BAE Systems has revealed that it is adapting cutting-edge bone conduction technology for Land Rover BAR's world class sailing team, as it seeks to boost the team's bid to bring the America's Cup home to Britain in 2017.

Global Military Radars Market to Reach $13.04B by 2020

The global military radars market was valued at USD 11.02 billion in 2015 and is projected to reach USD 13.04 billion by 2020, at a CAGR of 3.42% from 2015 to 2020.

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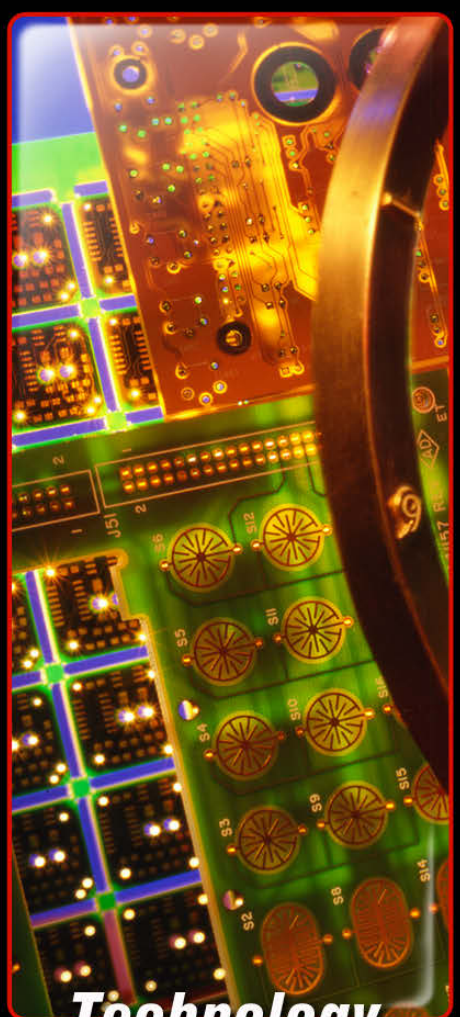

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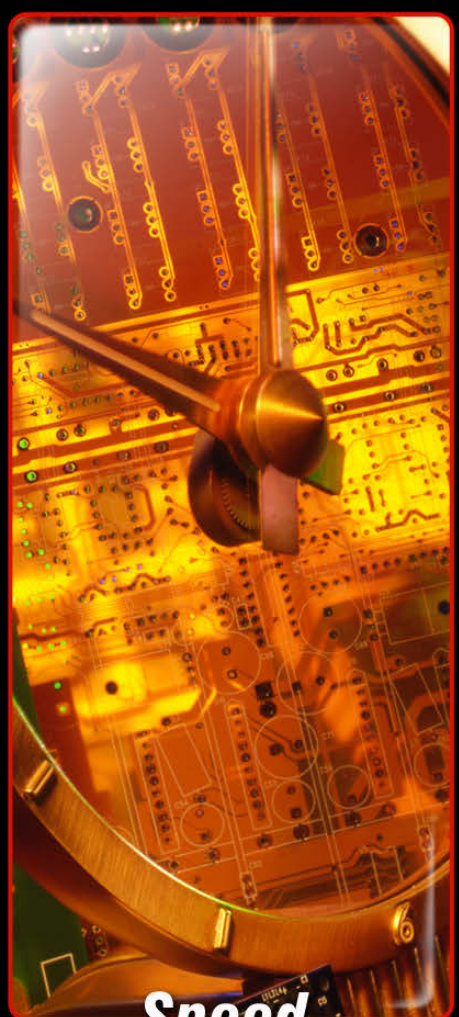

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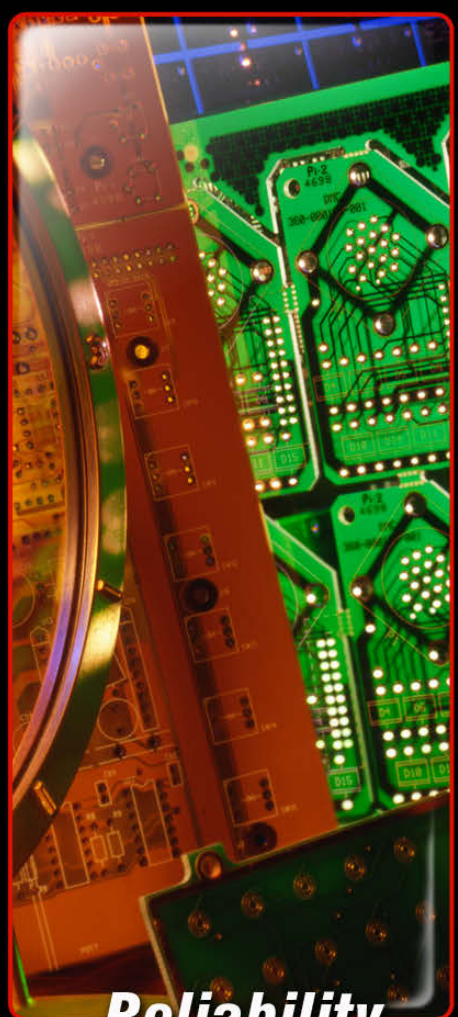

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Designing for Profitability:
Don't Over-materialize

by Barry Matties

John Bushie, applications engineering manager at ASC, explained to me recently about how designers can avoid over-materializing. He also outlined the benefits of designing for profitability.

Barry Matties: *John, what does it mean to be an applications engineering manager for American Standard?*

John Bushie: I work with customers to select the correct materials and structures for realizing their circuit board designs.

Matties: *For context, tell me about American Standard and what the company does.*

Bushie: We specialize in a wide variety of circuit board applications. We deal in the DC to 100 gigahertz range, and that means we work with conventional materials like FR4, but we also get into the more exotic and extraordinary materials, like the very low-loss PTFEs, polyimide materials, Megtron 6, as well as materials that are designed specifically for more commercial LED products, like IMS or MCPCB applications.

John Bushie

Matties: *In your position as the application engineering manager, you must see a lot of interesting challenges.*

Bushie: We do, and a lot of our expertise is brought to bear on bringing solutions to our customers. Examples are mixed dielectric metal core boards for Locomotive fuel injection to satellite based telecommunications using hybrid aluminum backed materials.

Matties: *What's the most interesting challenge that you've come across, that you can recall?*

Bushie: We deal with so many on a regular basis that it's difficult to answer that question. The hybrid aluminum-backed PCB was extremely challenging.

Matties: *Is there one that is a repeating challenge?*

Bushie: I can answer that question quite simply. While this sample board I'm holding is commonplace for us nowadays, it was quite challenging developing the process and control procedures that allow this unusual board to be readily manufactured. This is a vehicular collision-avoidance board, which is a 24 gigahertz

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application. Now it doesn't seem like much, and despite the fact that we produce 20,000 of these a week, it's a very unique board design. It ends up with four different materials combined into a structure that has a transmit and receive portion of a radar system. This is basically a compact portable radar system, which is used in automotive applications for either intelligent cruise control or, in this case, where it's simply used to detect near objects. This is unique in that it uses an RF material on the top, it uses a standard FR-4 circuit board material as basically an air spacer, and another slightly lower loss RF grade FR-4 simply as the antenna portion. Not to get into too much detail about this, but this seemingly simple board has many years of development into making it a relatively simple and manufacturable design.

***Matties:** One of the things that I hear frequently is people over-materializing their boards, and this sounds like an application where you're not doing that; in fact, you're doing exactly the opposite.*

Bushie: You have to in these types of applications that turn into large volume, commercial products. There are applications where cost is no object. This other particular board, for instance, is actually a satellite application, and this uses the same or very similar RF material as this board. Whereas this might be a $7 circuit board, this might be 100 times that. This is a unique combination of aluminum, Rogers 4000 series product, and polyimide, all bonded into one simple structure. By taking the alternative approach and consistently evaluating the cost of all base components and process options, we are able to manufacture the most performance for the minimum cost.

***Matties:** You deal primarily with a lot of designers and when a designer is coming in, what is it that they really need to know to be successful at creating a design that's going to go through and provide the result that they're anticipating?*

Bushie: What they need to know is that we're really there to act as their materials and design resource. We like to have a very close working relationship with the engineers, because we can help them make not only a very cost-effective product, but something that can be reproduced simply and readily.

***Matties:** Shouldn't the designers know some of this already and come to you and say, "This is what we're looking for?"*

Bushie: They do a lot of times, and while we're certainly not designing it, what we're helping them to do is to tweak and adjust certain portions of their structures, which may allow them to use slightly lower-cost materials and realize an ultimately lower-cost product.

***Matties:** One of the things that we see in design is design for manufacturability, and there's also a profit element, what we call DFP, design for profitability. When we look at the multiple uses and the range of materials now, that has to be taken into consideration, as well. It's the profit that you can get out of a board by a smarter design too, right?*

Bushie: We want to build the value into the board, and a lot of times we can do that by the design aspect instead of simply just putting

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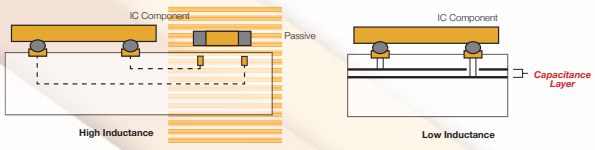

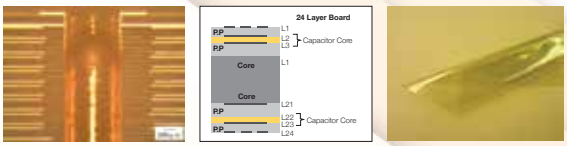

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all the money into materials or process time. Meaning, you can make a board on the best RF materials and be very successful, but what we're trying to do is balance the trade-offs. What can we do to reduce the costs while still achieving the results you're looking for? I believe that this objective has to be the goal of the fabricator as well?

***Matties:** From a technical point-of-view, where do you see the market headed?*

Bushie: We see it headed to lower and lower cost materials. We see higher levels of integration, and I almost always use that when I have these types of interviews, but the reality is everybody wants their package to do more. They want to put more stuff in a smaller box. Ultimately, that means we're bringing various circuit aspects together, or system aspects together into one combined technology.

***Matties:** What's your background?*

Bushie: My background is actually from the circuit board world. I started out at a fabricator, but quickly moved into the low-loss RF PTFE-based materials. I worked for a laminate supplier for many years, and then ended up getting back into the circuit board world to do what I enjoy, which is working with engineers developing these types of interesting products.

***Matties:** Is there anything that we haven't talked about that we should share with designers?*

Bushie: Get us involved as soon as possible. Meaning, the earlier in the design stage that you can begin working with your fabricator, the better. Because they can help you realize or find pitfalls in a design before you get too far along in the prototyping or initial design stages.

***Matties:** Great advice. We appreciate you taking the time to talk to us. Thank you so much.*

Bushie: Thank you very much. **PCBDESIGN**

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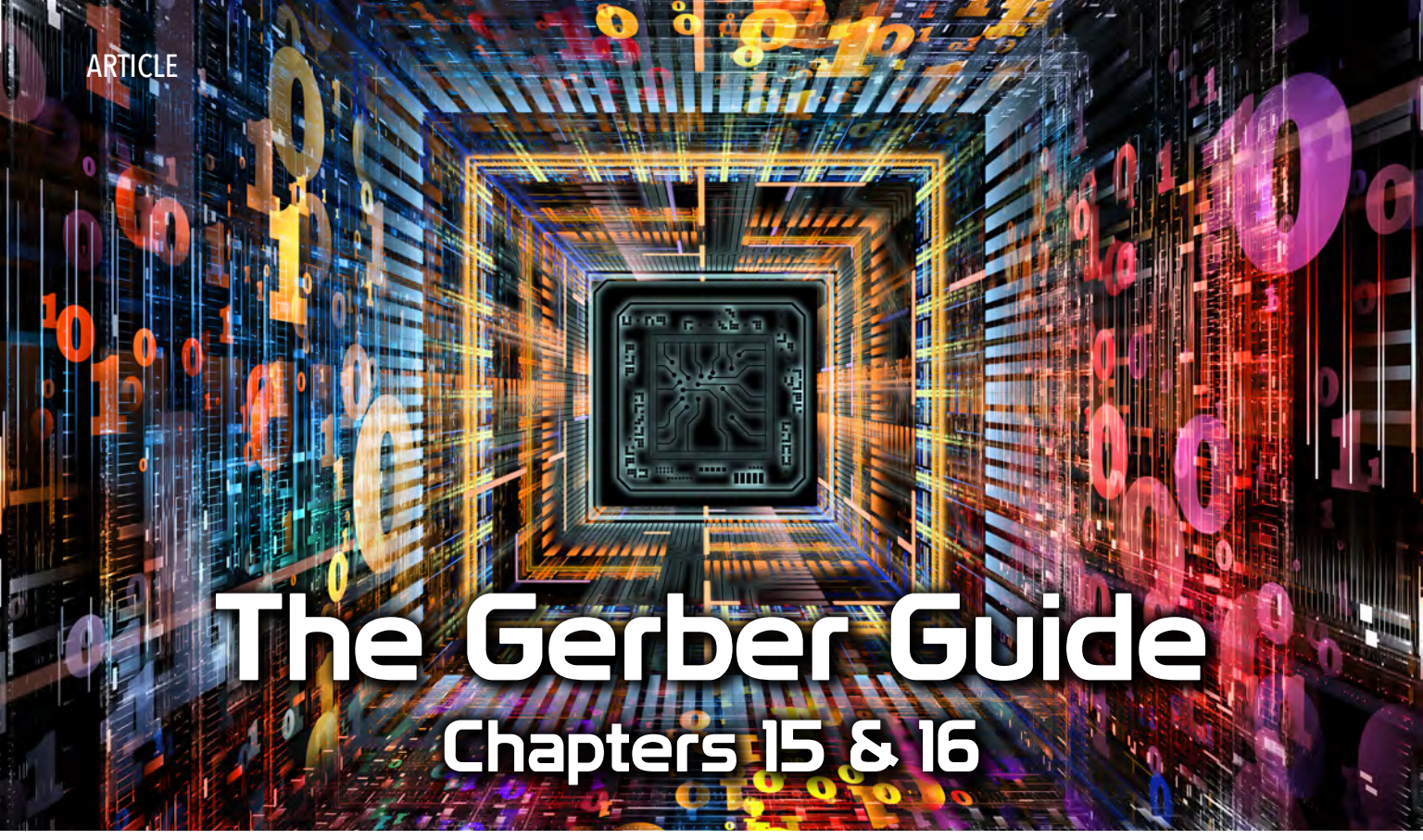


The Gerber Guide

Chapters 15 & 16

by Karel Tavernier
UCAMCO

It is possible to fabricate PCBs from the fabrication data sets currently being used; it's being done innumerable times every day, all over the globe. But is it being done in an efficient, reliable, automated and standardized manner? At this moment in time, the honest answer is no, because there is plenty of room for improvement in the way in which PCB fabrication data is currently transferred from design to fabrication.

This is not about the Gerber format, which is used for more than 90% of the world's PCB production.There are very rarely problems with Gerber files themselves; they allow images to be transferred without a hitch. In fact, the Gerber format is part of the solution, given that it is the most reliable option in this field. The problems actually lie in which images are transferred, how the format is used and, more often, in how it is not used.

Each month we look at a different aspect of the design to fabrication data transfer process. In this monthly column, Karel Tavernier explains in detail how to use the newly revised Gerber data format to communicate with your fabrication partners clearly and simply, using an unequivocal yet versatile language that enables you and them to get the very best out of your design data.

Chapter 15: The Use of Gerber Viewers

Before sending your Gerber files off to your fabricator, you are often advised to check them using a reputable Gerber viewer such as GC-Prevue. This is excellent advice.

Note that this involves more than just verifying that the viewer displays your intended image: It is important that you check too that the file is valid. Even when handling invalid data, viewers typically try to reverse engineer the intended image by 'reading between the lines'. This is perfectly OK, but the file is still invalid and, according to Gerber specification: An invalid Gerber file is meaningless and does not represent an image.

A file with errors must not be sent to the fabricator as if all is well, even if the intended image is shown. This is because even if *your reader* has reverse engineered the intended image from the invalid data, *another reader may not be so successful*. And that reader may be your fabricator's CAM, which will result in scrap. Should this happen, the fault lies squarely with

the file. To quote from the Gerber specification: The responsibilities are obvious and plain. Writers must write valid and robust files and readers must process such files correctly. Writers are not responsible for navigating around problems in the readers, nor are readers responsible for solving problems in the writers.

It is therefore extremely important that you check that your files are valid. Invalid files can cause viewers to throw error messages like the one in Figure 1, taken from GC-Prevue:

These messages clearly indicate that there is something very wrong with the file. The question is, what you do if you see such errors? It's not easy. Low resolution is often the root cause of problems, so it is worth trying to output the file at the resolution recommended in Chapter 10 in this series.

The only safe solution is to fix the bugs in the Gerber output software. It is therefore essential that you provide detailed information of the problem to your software supplier so that the bug can be fixed for the future. That said, the chances are that your board cannot wait for this fix and you have no way to output a valid file. This is then a conundrum. You could send the invalid data with the necessary caveats and hope that your fabricator's software, like your reader, will reverse engineer the intended image correctly. If it does, all is well. But this is a risk, so if you decide to do this, always include a netlist as a safeguard, as advised in Chapter 8 in this series. You can also ask your fabricator to send you the images he generates in CAM, so that you can check them for errors.

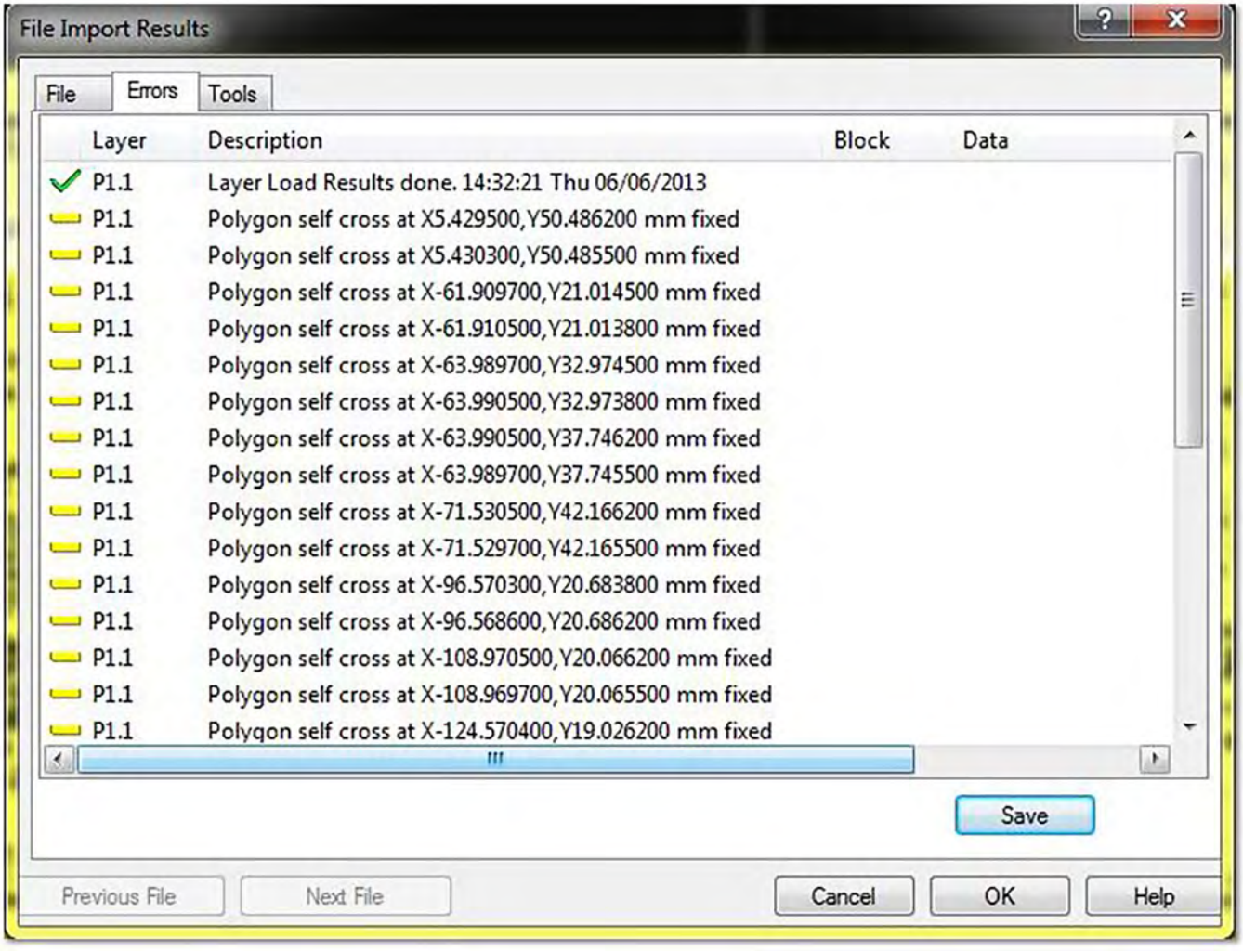


Figure 1: Error messages in a viewer.

Check the error messages of your Gerber viewer and act on them.

Chapter 16: Standard Gerber

To quote from the Gerber format specification:

Standard Gerber is revoked and superseded by Extended Gerber, which is the current Gerber format. Consequently, Standard Gerber no longer complies with the Gerber specification. Files in that format can no longer be correctly called Gerber files. Standard Gerber files are not only deprecated, they are no longer valid.

Please use Extended Gerber for all of your operations. Standard Gerber is technically obsolete. If you are still using it, you are putting your business and that of your clients and business partners at a useless risk, without benefit.

Despite its name, Standard Gerber is not a defined standard for PCB data transfer: Units and aperture definitions, rather than being governed by a recognizable standard, are in an informal document, the interpretation of which is unavoidably subjective. As a result, Standard Gerber files cannot be machine-read in a standardized, reliable way.

Standard Gerber requires aperture painting and copper pours, both of which create manual work in CAM, adding cost, delay and risk to the PCB manufacturing process.

Standard Gerber does not support attributes.

Extended Gerber files *are* machine readable, they do *not* require painting, and they *do* support attributes. Virtually all software reads Extended Gerber and many new implementations no longer support Standard Gerber. There is not a single good reason left to use Standard Gerber. The use of Standard rather than Extended Gerber is a self-inflicted competitive disadvantage.

To quote from the specification once more:

Warning: The responsibility of errors or misunderstandings about the wheel file when processing a Standard Gerber file rests solely with the party that decided to use revoked Standard Gerber, with its informal and non-standardized wheel file, rather than Extended Gerber, which is unequivocally and formally standardized.

More information can be found in the Open Letter on Standard Gerber, which is on the download page at www.ucamco.com. **PCBDESIGN**

This column has been excerpted from the Guide to PCB Fabrication Data: Design to Fabrication Data Transfer.

Karel Tavernier is the managing director of Ucamco.

From Battery Cell to Battery Pack Components, Companies are Seeking Better Margins

Battery pack components are gaining importance in the fast-growing battery pack market, reaching US$65.7 billion by 2021. Yole Développement (Yole) pursues its exploration of the battery world and releases this year in a new report "Stationary storage & Automotive Li-ion battery packs."

The battery pack is the key element of battery storage systems. Such systems are used for clean mobility in hybrid electric vehicles and battery electric vehicles, and are crucial for the further deployment of intermittent renewable energy sources like wind and photovoltaics.

A main part of the battery pack demand will come from the automotive industry. In 2015 the demand in MWh for plug-in hybrid electric and battery electric vehicles was about 18x higher than for stationary applications. This ratio will remain almost unchanged by 2021 because both the automotive and stationary markets will feature strong growth. Today, the development of innovative battery technologies is focused mainly on battery cells as a key component of the battery pack. In fact, cells represent more than 50% of the battery pack cost.

TOP TEN

Recent Highlights from PCBDesign007

1 PCBDesign007 to Launch "Design Tips" Feature

PCBDesign007 will soon launch Design Tips, an ongoing feature that will be driven solely by input from PCB designers and design engineers. All you have to do is send us your favorite design tips, tricks and techniques. This information can encompass any area of PCB design or design engineering.

2 Beyond Design: The Case for Artificial Intelligence in EDA Tools

There has been a lot of activity in the field of artificial intelligence recently, with such developments as voice recognition, unmanned autonomous vehicles and data mining to list a few. But how could AI possibly influence the PCB design process? This month, Barry Olney will take a look at the endless possibilities.

3 The Importance of Design for Profit (DFP)

In this interview, Interconnect Design Solutions' Mike Brown and Barry Matties took a few minutes during the recent Geek-A-Palooza event to discuss the importance of material selection and designing for profitability, how automation affects the design process, and the future of the design community.

4 Changing the World of PCB Rapid Prototyping

Tony Tung is a recent graduate from Taiwan who has come up with a new way for PCB designers and makers to create breadboards using printed paper circuits. I caught up with Tony at the recent San Mateo Maker Faire and sat down with him to learn more about this project.

5 Ucamco Seeks Comments on Gerber Nested Blocks Capabilities

Ucamco welcomes designers' input on its latest proposal: to extend the Gerber format with nested blocks capabilities. The principal aim in doing so is to make panel definition and handling easier and more efficient, and it is most likely that this development will bring additional benefits. Before this goes live, the company asks Gerber users to read the proposed new draft specification.

6 The State of the Electronic Design Automation Nation

We are the automation nation. We are the high-speed demons, the low-frequency artists, the mixed-signal designers that make up the electronic design automation industry. We spend most of our working lives behind software, delivered to our fingertips with the promise of making things easier, faster, better, and getting us to our deadlines ever faster.

7 Rogers' John Coonrod on Insertion Loss

John Coonrod of Rogers Corporation gave a keynote presentation at the recent Geek-A-Palooza trade show, concentrating on printed circuit board fabrication's influences on insertion loss. I sat down with John to learn more about his presentation and what OEMs and designers need to be aware of to avoid insertion loss.

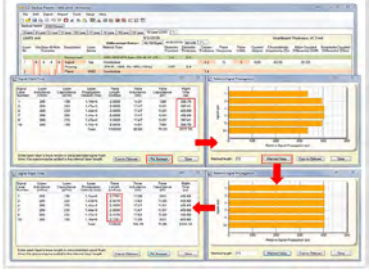
8 Zuken Launches Latest Version of E3.series Software

The E3.series 2016 has been enhanced to offer a smoother user experience for today's globally dispersed design teams. Users can work simultaneously on one sheet and instantly see in the sheet tree if another user has opened it, as their user name is visible.

9 Tim's Takeaways: The Basics of Hybrid Design, Part 3

We are seeing more and more of our customers exploring the world of hybrid design, and we are getting new customers for whom hybrid design is their sole focus. And yet many designers out there (and I used to be one of them) have no idea what is meant when people start talking about hybrid design.

10 ICD Adds Matched Delay Optimization to Stackup Planner



In-Circuit Design Pty Ltd (ICD), Australia, developer of the ICD Stackup and PDN Planner software, has released a Matched Delay Optimization feature for the Stackup Planner. This allows you to automatically calculate the appropriate length required to match the delay exactly.

PCBDesign007.com for the latest circuit design news and information—anywhere, anytime.

Events

For IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out The PCB Design Magazine's event calendar.

IPCA EXPO 2016
August 18–20, 2016
Delhi, India

PCB West
September 13–15, 2016
Santa Clara, California, USA

Medical Electronics Symposium
September 14–15, 2016
Marylhurst, Oregon, USA

24th FED Conference
September 15–16, 2016
Bonn, Germany

IPC India/electronica India 2016/ productronica India 2016
September 21–23, 2016
Bengaluru, India

IPC Fall Committee Meetings
September 24–30, 2016
Rosemont, Illinois, USA

SMTA International 2016
September 25–29, 2016
Rosemont, Illinois, USA

electronicAsia
October 13–16, 2016
Hong Kong

TPCA Show 2016
October 26–28, 2016
Taipei, Taiwan

Electronica
November 8–11, 2016
Munich, Germany

FUTURECAR: New Era of Automotive Electronics Workshop
November 9–10, 2016
Atlanta, Georgia, USA

International Printed Circuit & Apex South China Fair (HKPCA)
December 7–9, 2016
Shenzhen, China

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